The Design of PPM Modulation System Based on Fiber Laser

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Abstract. The advantages of fiber laser are its high gain, low threshold, high conversion efficiency, its good output beam quality, simple structure, line width and high reliability. PPM (Pulse Position Modulation) modulation has higher peak power and lower average power, a higher signal to noise ratio and covert security features. This fiber laser PPM modulation system design is important for laser communication. This paper designs hardware circuit of PPM modulation system, and it uses TMS320VC5402 modulator. The experimental results show that the PPM modulation/demodulation system is reliable, logical relationship is correct, it can achieve information modulation for fiber laser communications perfectly.

Keywords: Fiber lasers; PPM; modulator.

1. Introduction

Atmosphere laser communication system consists of two sets of laser communication machines, they emit modulated laser impulse signals (data or voice) to each other, to receive and demodulate the laser impulse signals from each other, to realize the duplex communication. There are some key technologies in free space laser communication: a precise and rapid acquisition, tracking and pointing (ATP) technology [1], high power laser, atmospheric channel, precise and reliable high gain, antenna etc. The fiber laser with its unique superiority in free space laser communication is used more and more widely, its advantages are mainly embodied in: high gain, low threshold, high conversion efficiency, good beam quality, simple structure, narrow linewidth, and high reliability, and it is the structure of guided wave, which can hold strong pumping, easy to realize the fiber coupling. The progress of technology, especially when optical fiber devices based on the filter, fiber grating, fiber optic technology are coming to market, will provide new ideas and strategies for the design of fiber laser. The market of cladding pumping fiber laser, 3lRFL and 2lRFL, undoubtedly reflects the enormous potential of fiber laser.

The PPM uses pulse' relative position to transmit information, and it only controls pulse position according to the data symbol, without the need for controlling pulse amplitude and polarity. Compared with other OOK modulation, PPM modulation has high peak power and low average power, high signal-to-noise ratio and safety hidden characteristics. It has low implementation complexity of modulation and demodulation, and it is widely used in the field of optical communication technology, ultra wide band mobile communications and other modern communication frontiers. In addition, PPM also has a good prospect of application in the long-distance communication, optical soliton communication and underwater communication optical fiber, with commercial and defense significance.

2. PPM Modulation system principles

The hardware design of system is shown in the following diagram, which can meet the requirement of the system performance index.

The principle of the system is the realization of the signal processing interface information through the information processing unit into a binary data stream, in accordance with the needs of the PPM modulation system. We encodes the L bit binary information for a PWM pulse, and the modulated PWM pulse sequence is sent to the PPM output unit, a trigger to generate PPM pulse sequence, then

the PPM narrow pulse goes through the driving circuit of laser to modulate laser, and finally sent into the atmosphere channel by the optical system.

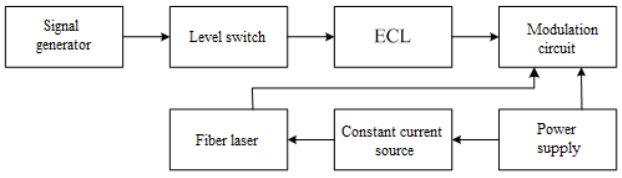

Figure 1 Diagram of hardware system design

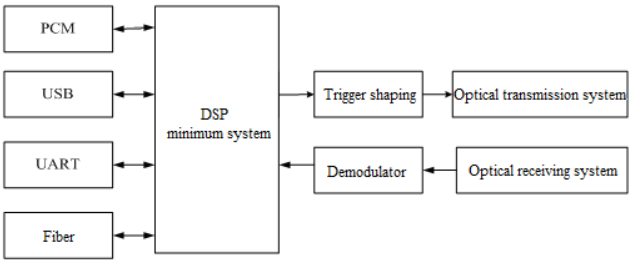

Figure 2 Diagram of hardware system

3. The design of PPM modulation system

This section introduces the design of the 16-PPM modulation based on TMS320VC5402 modulator. The system hardware block diagram is as shown below. The laser communication system has asynchronous serial interface, telephone audio interface, universal serial bus interface and optical interface, four interfaces to exchange information with the outside. This paper only uses asynchronous serial interface of computer performance, RS232 communication interface to verify the function of modulation and demodulation system.

3.1. The DSP minimum hardware system

A DSP hardware system consists of the minimum hardware system and peripheral interface. The system uses TMS320VC5402 as the control circuit, including the clock circuit, reset circuit, power management circuit, extended memory circuit, a state indicating circuit, and JTAG interface circuit simulation.

3.1.1 The power management circuit

The power management circuit design mainly focuses on three aspects: the order of supplying power, the requirement of electric current and the structure of power supply voltage, and it provides power for the system DSP chip and other components

TMS320VC5402 works with low voltage, and the I/O pin voltage is 3.3V, and the core voltage is 1.8V. But the peripheral device working voltage is 5V, therefore, the power management circuit provides 3 voltages: 5V, 3.3 V, 1.8 V. The common DC voltage is 5V or higher, so we must adopt a voltage conversion chip to convert the high voltage into 3.3 V and 1.8V. At the same time, the system current mainly depends on the device's activation. The I/O pin current depends on the external interface pin activation, while the kernel current depends on the CPU activation. In addition, in the ideal condition, the sequence of DSP chip power supply pin is simultaneous. At the same time it can not be absolute, we shall ensure that the I/O pin is get the power before the kernel power.

This paper chooses the voltage conversion chip TPS73HD318 of TI Company, and it will change 5V to 3.3 V and 1.8V. The maximum output current is 750mA; power supply circuit is shown in figure 3.

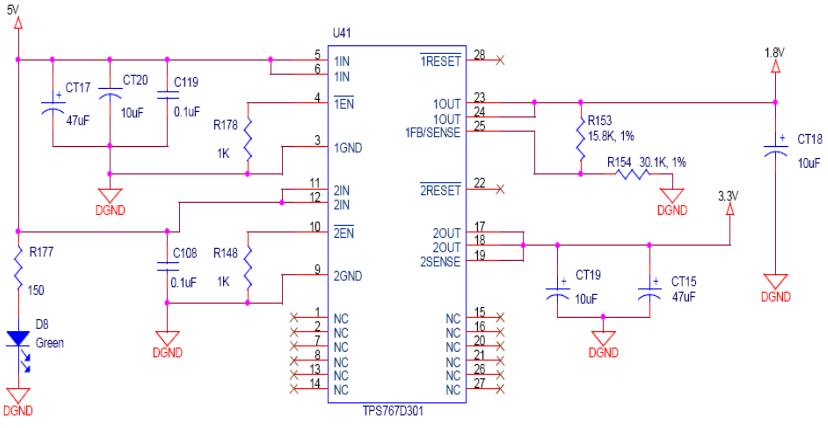

Figure 3 Power circuit

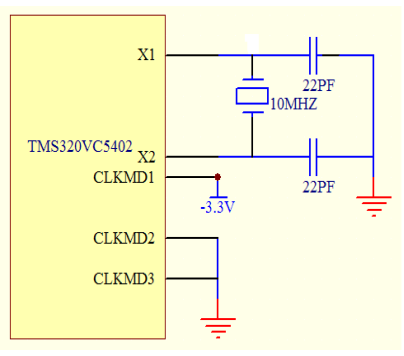

Figure 4 Clock circuit

3.1.2 The clock circuit

The system needs a work rhythm, the rhythm is provided by the clock circuit. Crystal or oscillator is two ways to provide an external reference clock signal TMS320VC5402. When the re. When they require a plurality of different frequency clock signals in the system, we prefer oscillator, where the X1 pin is suspended, and the oscillator output is connected to the X2/CLKIN pin; when the signal uses a single clock system, can choose the passive crystal, we will connect pin of crystals with Xl and X2/CLKIN pin of TMS320VC5402. Due to the higher internal instruction cycle of TMS320VC5402, TMS320VC5402 internal phase lock loop (PLL) circuit make the working clock frequency 0.25-15 times the external reference clock, which reduce the external clock frequency and improve the stability of the system. PLL clock has two modes: hardware configuration and software configuration. Hardware configuration refers to the system reset, automatic detection CLKMD1, CLKMD2, CLKMD3 three pin state of TMS320VC5402 by CPU, to determine the relationship between working clock and an external reference clock multiplier. Software configuration refers to the system after reset, adjusts the clock frequency of the CLKMD register by way of the software to change the PLL contents.

According to the above analysis, we can set the system clock is 24MHz, and choose a clock circuit with passive 12MHz crystals. CLKMD1, CLKMD2, CLKMD3 pin of TMS320VC5402 are respectively arranged at a high level, low level, low level, so the work frequency is 24MHz when the system is reset, which is two times the external reference clock source (12MHz).

3.1.3 Reset Circuit

The reset circuit is a circuit required by the minimum system, and the reset circuit can output stable reset signals. TMS320VC5402 has 3 modes of reset: power reset, manual reset, software reset. The first two are reset by hardware circuit implementation, the last one is reset by instruction mode. In addition, the system is vulnerable to outside interference: when the power supply fluctuates, it is prone to break down. Therefore, the design of hardware reset circuit of the utility should consider the convenient operation, reliable work and other factors.

RESETT is a TMS320VC5402 reset pin, which is active when the voltage is low. The system is installed with a power source monitoring circuit, which can guarantee the DSP chip will not be out of control when the power supply does not meet the requirements of the level. The power reset circuit is a commonly used reset circuit. When the power is on, it will produce a low level signal (100~200ms), which initializes the system chip. In this paper, the power chip of power supply circuit has a power supply monitoring and reset management function, and the reset circuit design is very easy.

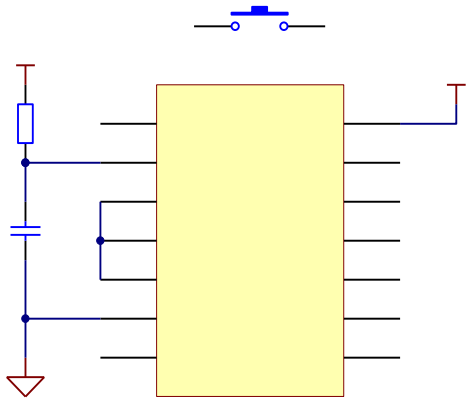

Figure 5 Reset circuit

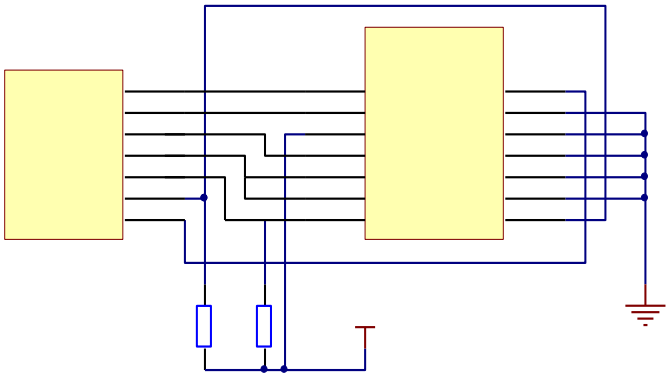

Figure 6 JTAG interface circuit

3.1.4. The JTAG interface circuit

The JTAG interface is a standard interface which satisfies IEEE Std 1149.1 boundary scan logic standard. It is mainly used for real-time online simulation test in the hardware and a DSP program download. It not only provides the boundary scan for the connected device, but also can be used to test the pin to pin continuity, and chip operation test of DSP's peripheral device. Almost all high speed controller and programmable device need JTAG. This paper designs 14 pin socket standard interface

the JTAG, which can be used for debugging emulator. Pin's definition of the JTAG interface cannot be changed freely as it is an industry standard. Specific connection is shown in figure 7. TMS320VC5402 provides the JTAG interface chip, which is convenient to debug. We only need to connect 7 pins: TMS, TDI, TDO, TRST, TICK, EMU0, EMUI of TMS320VC5402 to make a standard 14 pin socket, and then we can debug the system board.

When the link length of cable between the simulator and the system board does not exceed 6 inches, JTAG and TMS320VC5402 interface is shown below. When the link length of cable between the simulator and the TMS320VC5402 is more than 6 inches, we need to install driving device in data transmission line. Among them, EMU0 and EMU1 is the simulation signal pin, which must be connected by a pull-up resistor to VCC, to provide less than 10us of the signal rise time, while ensuring that the signal's high quality between the simulator and the JTAG target system.

3.2 Circuit of asynchronous serial interface

TMS320VC5402 chip has 2-3 full duplex, high speed, multi-channel buffered serial port (McBSP), and it can be used with most synchronous serial peripheral interface. McBSP is based on the standard serial interface to extend the functionality, which features standard serial port.

Considering the convenience of the hardware connection and software programming, we use the MAX3111 asynchronous serial transceiver of American MAXIM company, to directly connect with the DSP's port McBSP. The hardware has any other peripheral device, at the same time as the transmission of asynchronous data and receiving by MAX3111 is realized by hardware, software programming only needs to consider the synchronization of data communication between DSP and MAX3111. So we can realize synchronous to asynchronous serial data format conversion by connecting the hardware and software programming.

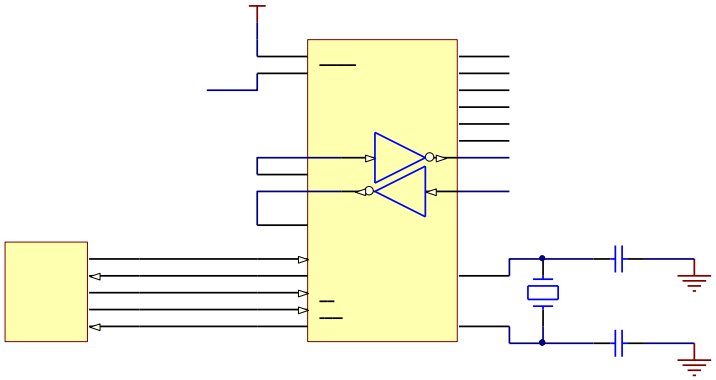

Figure 7 Circuit of asynchronous serial interface

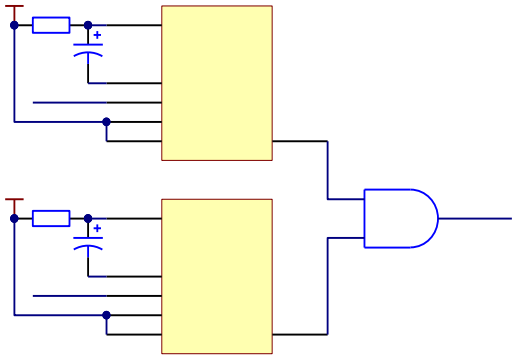

Figure 8 PPM narrow pulse generate circuit

3.3 Trigger shaping circuit

Trigger shaping circuit is composed of the gate circuit and monostable trigger 74HC221 which can not be repeatedly multivibrated, whose role is to trigger PPM narrow pulse, thus modulated laser. PWM wave generated by DSP are fed into a trigger shaping circuit made up by 74HC08 and two triggers 74HC221. The trigger principle is the decreased PWM wave drops along triggered PPM narrow pulse, which can generate the needed PPM pulse signal. Circuit implementation is as follows.

The two triggers 74HC221 are used to generate PPM narrow pulse, which can avoid the risk and competition, and make the PPM more precise. While it is more convenient and accurate for the TMS320VC5402 to encode PWM wave, and the PWM waves generated by the hardware circuit can be converted to PPM pulse, thereby realizing PPM modulation.

4. System simulation

After the initial completion of algorithm design, we realize the system simulation by software. Through the oscilloscope, the oscilloscope displays random binary information input waveform as is shown in Figure 9, and the simulation of PPM modulation system is shown in Figure 10.

Figure 9 Input signal waveform

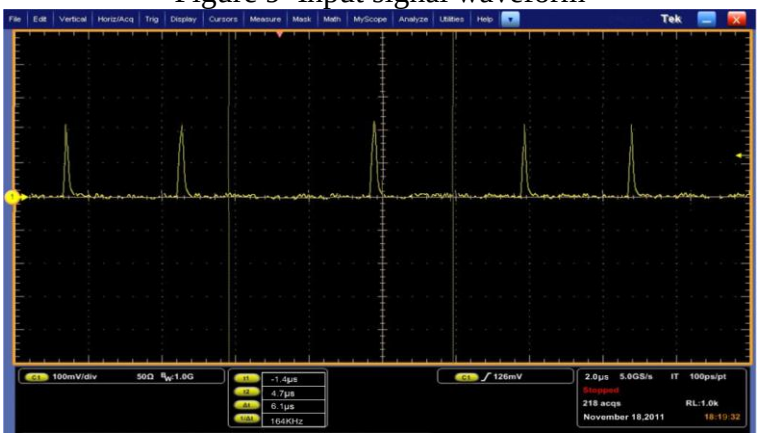

Figure 10 Simulation results

Conclusions

In order to ensure the data error rate and bit rate, we set the present goal as to reduce power loss as far as possible, and to take into account the laser's characteristics of the laser emission, and the feasibility in the actual system of space laser communication system. PPM modulation simulation system has finished loading modulation signal, and established the foundation for the further research of the transmission loss of optical signals in the atmosphere, thus performance of the space optical communication system can be evaluated. For the optical wireless communication system, it is an important simulation interface module. The experimental results show that the PPM modulation system is reliable and it has correct logical relationship, which can complete the information modulation of fiber optical communication.

References

[1] Zhou Yamin, Liu Qizhong, Zhang Xiaohui, et al. Study on demodulation methods for underwater laser stretched pulse PPM signal. optical technique, 2011, 36(1): 88.

[2] Zhang Huawei, Jia Honghui, Yin Hongwei, et al. The analysis of L-PPM modulation for ultraviolet laser communication. optical communication technology, 2010 (005): 56-58.

[3] He Pan, Li Xiaoyi, Hou Qian, et al. Design of PPM modulation and demodulation system based on FPGA. Modern electronic technology, 2010, 33(009): 52-54.

[4] Malina. PPM modulation of polarization and its experiment research in atmospheric laser communication. Xi'an University of Technology, 2009.

[5] He Xiaozhe, Zhang Hao. On Capacity of 60 GHz Wireless Communications System with Pulse Position Modulation Abstract. China new technology and new products, 2011, 10: 028.

[6] Mu H, Yao J. Photonic generation of UWB pulses with pulse position modulation. Electronics le tters, 2010, 46(1): 99-100.