The Design of High Frame Rate Linear CCD Data Acquisition System Based On USB 2.0 Interface

Yingzhi Wang[1], Han Lin[2], Zewen Chang[3], Jia Yang[4]

[1] Changchun University of Science and Technology, Changchun 130022 China

[2] School of Electronics and Information Engineering of Changchun University of Science and Technology Class 1304113, Changchun 130022 China

[3] School of Electronics and Information Engineering of Changchun University of Science and Technology Class 1304111, Changchun 130022 China

[4] Jilin Jianzhu University, Changchun 130118, China

Abstract

With the development of semiconductor technology and the wide application of data acquisition system, people have a higher requirement of CCD image acquisition system. Because time consuming of the data processing limits the measurement speed of system, the traditional CCD image acquisition system can't satisfy the recognition of dynamic target and the requirement of the rapid real- time detection. This article designed a kind of high speed linear CCD signal acquisition system. This system adopts the scheme that the USB2.0 interface control chip combined with FPGA. There are many characteristics, such as, low power consumption, high clock frequency, high speed, high efficiency and flexible combination, etc. Design and implement a high speed linear CCD data acquisition system based on USB2.0 interface. Test results show that the acquisition rate of the system can reach to 7500 frames per second and USB transmission rate can reach to 200 Mbps.

Keywords

linear CCD; USB2.0; FPGA; data acquisition.

1. Introduction

CCD converts light signal into charge signal and output every picture element one by one, it features high accuracy and sensetivity, wide optical spectrum bandwidth with low noise. [1] In practice measure, there are two kinds of CCD, they are linear array CCD and area array CCD, the key of this design is to acquire and process the signal from linear CCD. [2]

In the CCD signal acquiring and processing system, If make MCU to be the controller to acquire and process data discontinuously, the processing speed will be very slow, the real-time effect is not ideal enough; if we transmit data through DMA channel to the upper computer and make PC to process the data it acquires, the cost of resource is too much. [3] In this article, we will introduce a high frame rate linear CCD signal acquiring and processing device , it is comprised of A/D converter, FPGA and USB2.0 interface IC, this device is perfect for high speed, real time data acquiring, and the effect of processing is great.

2. Overall Design Scheme

According to the function of this system, the design of the hardware part in this system includes the linear CCD, signal processing circuit, A/D conversion circuit, FPGA and USB2.0 interface chip. System adopts the programmable logic device FPGA control timing sequence of the linear CCD and sampling of A/D converter at the same time, Using FPGA internal cache FIFO to complete data buffer and high speed data transmission of USB Controller. The reprogrammable feature of FPGA improves the working efficiency and flexibility of the design. What's more, using the hardware description language to describe hardware makes hardware design as flexible as software. The firmware program

of USB2.0 interface chip CY7C68013A is stored in EEPROM. EEPROM and CY7C68013A are connected through the I^2C interface. CY7C68013A will download program automatically to the internal RAM from EEPROM after it powering on, then USB enumeration and the firmware program will start. The overall design scheme of the system as shown in fig.1.

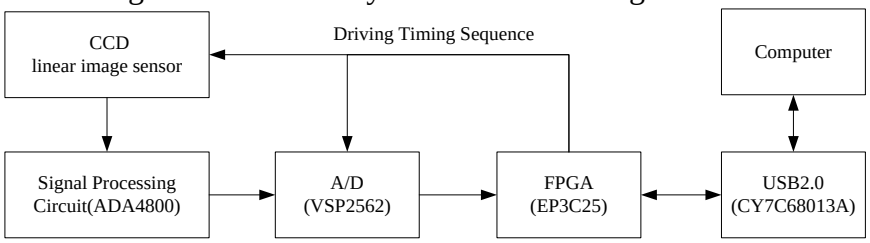

Fig.1 Structure diagram of the Overall Plan

The whole working process of the hardware circuit: when the upper computer sends the request of data acquisition, FPGA begin to control timing sequence of the linear CCD and sampling of A/D converter. Using FPGA to send the A/D conversion data to USB2.0 controller. Then the data is transmitted to the upper computer through the USB bus.

3. Hardware Design and Implementation

3.1 Linear CCD

Select TCD1209D of the TOSHIBA, it is a high speed, low dark current, PDIP22 device. It can be used for spectral analysis, facsimile, image scanning and optical character recognition, etc. It contains 2088 high sensitivity P-N junction photodiodes. The length of photo-sensitive has 28.6mm.

TCD1209D contains 2088 high sensitivity p-n junction photodiodes constituted array of photo-sensitive elements that have length of 28.6 mm. The CCD has 2048 pixels, because the array of photo-sensitive elements have only 2048 photodiodes which are exposed photo-sensitive unit, the array's front 32 and rear 8 which are used as dark current detection are shielded. The best working frequency of TCD1209D is 1MHz and the maximum drive frequency can reach to 20 MHZ. It mainly consists of two modules: surface photovoltaic conversion unit, shift register and output caching. The surface photovoltaic conversion unit is a pixel receive the light that is irradiated CCD silicon wafer and it is converted to charge signal. The size of electric charge depends on light intensity and integration time and it changes in a linear relation. The photoelectric signal charge of pixel via transfer gate and output from shifting register under the control of the given driving signal. The output caching is applied to convert charge signal into the voltage signal, and amplifies it. Finally, output it.

The best working frequency of TCD1209D is 1 MHZ and the maximum drive frequency can reach to 20 MHZ. Dynamic range is 2000. Sensitivity range from 25 to 37V/(lx. S) and its typical values is 31 v/(lx, s). The dark current voltage has inhomogeneous feature. Its typical value is 1 mV, its maximum value is 2.5 mV, typical value of saturating output voltage is 2 V and the minimum value is 1.5 V.

3.2 Signal Processing Circuit

The function of signal processing circuit is capture a weak input signal and process it appropriately. That make the voltage range of the input signal in our required limitation can meet input requirement of the A/D converter. This signal processing circuit uses the operational amplifier IC ADA4800.

The ADA4800 is voltage buffer integrated with an active load. The buffer is low power, high speed, low noise, high slew rate, fast settling, fixed gain of monolithic amplifier is 1, it is fit for charge-coupled device (CCD) applications. In CCD applications, the active load current source (IAL) can load the open source CCD sensor outputs and the buffer is able to drive the AFE load. The active load can also be switched off, and then ADA4800 as a unity gain buffer is used. The static power of the buffer only 20mW. In applications where power savings is critical, The ADA4800 provides a power save mode, which further reduces the total power consumption. The bandwidth of the ADA4800 is

also fully adjustable through the IDRV pin. The buffer of the ADA4800 employs a push-pull output stage architecture, which provides drive current and maximum slew capability at both rising and falling signal transitions time. At a 5mA quiescent current settling, it provides 400MHz-3dB bandwidth.

3.3 A/D Sampling Circuit

The main function of A/D converter chip is sampling, quantizing and encoding analog signal which has been processed, this system selects the VSP2562 of TI.

A/D converting circuit is a important part of this system. It decides the precision and speed of sampling. A/D is sampling the CCD signal that has been processed by ADA4800,it is a AM pulse which makes the CCD reset pulse to be the period, through impedance matching, gain control and related double sampling technology make the processing signal convert into digital signal.

VSP2562 is a 12-bits 36MSPS single channel analog front-end AFE, it has 2 CCD sensors of 8-bits DAC which can work under +3V supply. Including a related CDS, a PGA, a ADC, a input folder, OB Horizontal clamp cycle, a serial interface, timing control, and a reference voltage generator. Under different lighting condition, it has a very stable gain control range. The supply voltage of VSP2562 is 3V, its output capability is not strong enough, adding a buffer circuit when using it, now we choose SN74LVTH16244A to be the output data buffer.

3.4 The Design of FPGA's Internal Logic

The core of the control is FPGA in this system. FPGA provides a proper drive pulse of timing sequence and control A/D conversion work of CCD output signal. FPGA uses its internal FIFO (First In First Out) to buff sampled data and send the data to the USB controller.

FPGA uses EP3C24E144C8 of Cyclone III series, it has 24.624Les, 66 M9K RAM Blocks, the storage of RAM up to 0.6Mbits, suitable for video buffer; EP3C25E144C8 has 4 PLLs,144 Pins, there are 82 user I/O among them, EQFP package. Using EP3C25E144C8 to design, will enhance integration level, decrease power, shorten development cycle, satisfy the low-cost requirement at the same time.

(1)Design of CCD Driving Timing Sequence

To make CCD work normally it needs a driver, TCD1209D needs 5 channel pulses to control it. These five channel pulses are transfer pulse SH, drive pulse CR and CRS, reset pulse RS and buffer control pulse CPS.[4,5] The Timing Sequence Diagram Of TCD1209D Driving Pulse as shown in fig.2.

The output signal from FPGA is 3.3 V, but the drive signal of TCD1209D is 5V. So the output signal of the FPGA cannot be directly added to the CCD chip (TCD1209D). To solve this problem, it needs to add an additional peripheral circuit to improve the driving ability of the signal. To make TCD1209D work normally needs 6 channel drive signal which are Two-phase clock signal CLK1, CLK2, signal output clock signal CLK2B, pixel reset signal RS, transfer line sync signal SH, clamping gating signals CP. This system uses the inverse driver (SN74HC04) for driving timing sequential circuits of CCD. It can satisfy the signal level requirements of CCD and solve the problem which is drive capability of FPGA is insufficient. And the design of this circuit is simple. It can improve its reliability and reduce power consumption.

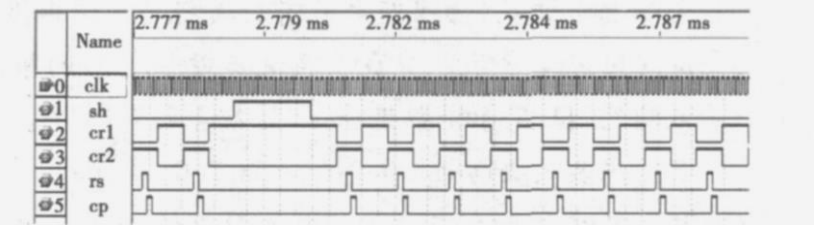

Fig.2 Timing Sequence Diagram of TCD1209D Driving Pulse

(2) Design of FIFO Data Buffer Module

In the FPGA image data processing, FIFO is used to cache the image data. FIFO is a kind of storage which has a special function. Its characteristic is first in first out. Due to the applications is so particularity that data needs to transmission and processing in real time. So every RAM of FIFO is working in the refresh - read - refresh cycle. It can obtain the better real time performance on the basis of sacrificing certain of logical resources. The Timing Sequence Diagram Of Slave FIFO Sync as shown in fig.3.

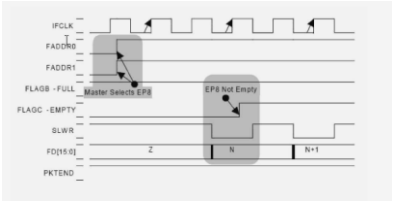

Fig.3 Timing Sequence Diagram Of Slave FIFO Sync

(3) Design of USB Interface Circuit

The working mode of USB controller is Slave FIFO synchronous mode. USB interface design in this article is the interface logic design between USB controller and FPGA. It's mainly FPGA sampling data through USB upload to PC in this system, which means FPGA write data to USB interface, by using Slave FIFO Sync write. The interface circuit between FPGA and USB is as shown in Fig.4.

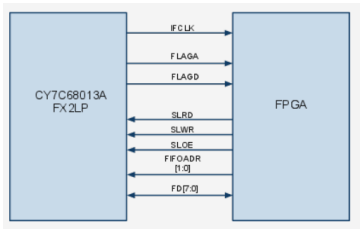

Fig.4 The Diagram of FPGA and USB Interface

Using state machine to make Slave FIFO Sync write in FPGA programming. As shown below are the states and its transitions.

IDLE: When the data in FIFO of FPGA has reached at a certain extent, writing event is triggered, jumped to STATEI;

STATE I: Transmission pointed to input port(the system configured EP6 as input port),active FIFOADR[1:0]to STATE 2;

STATE 2: Judge whether FIFO is full. If the FIFO is not full, turn the way to next state STATE3,or stop at STATE2;

STATE 3: Transmit data, active SLWR, turn to STATE4.

3.5 USB 2.0 Interface Circuit

CY7C6801A3 is a EZ-USB FX2 microprocessor that has USB2.0 core, 8051 compatible feature from Cypress. EZ-USB FX2 series IC is the microprocessor that earliest meet the standard of USB2.0, it supports 12Mb/s full speed transmission and 480Mb/s high speed transmission, integrated transceiver that accord with USB2.0 standard, serial interface engine, powered 8051 core, a 8.5K on chip RAM, a 4KB FIFO storage and a general purpose programmable interface.

3.6 Power Supply Circuit

Before the design of power supply circuit, you have to analyze the demand of every component in the system, the power circuit have to provide 5 kinds of DC powers to meet the demand of power in the system. The supply power for FPGA is 3.3v and 1.2V. The signal processing circuit is 15V. The supply power for A/D converter VSP2562 is 3.3V. The USB2.0 interface IC CY7C68013A needs 3.3V.

This design including several following circuits:

LD1117 low drop voltage regulator provides voltage that the system needs. In the range of rated working temperature, compared to normal voltage regulator IC, LD1117 is lower power and more

stable temperature characteristic. It can make over temperature and over flow protection efficiently. It has a broad application domain.it offers fixed voltage supply at: 1.2V, 1.5V, 1.8V, 2.5V, 3.3V, 5V. At the same time, it can also provide a adjustable voltage output (1.2V~VCC), by using 2 external resistors.

LT3023 has a stable 1uF output capacitor, input ranged from1.8V to 20V, output current: 100mA/channel, very low close the current current:<0.1uA, when the current is 100mA, the low differential voltage is 300mV,low noise:20u vrms (10Hz to 100Hz),low quiescent current(20uA/channel)makes it a ideal choice, adjustable voltage ranged from 1.22V to 20V.every channel has its own turn-off control, and flexible power supply management features.

LD1085 is a low drop voltage regulator which has a 3A output current. Three pins can be fixed to output or adjustable output ranged from 1.5V, 1.8V, 2.5V, 3.3V, 5V, 12V.

LT3436 is Linear Technology's 800KHz monolithic boost switching DC-DC power regulator. Input ranged widely from 3~25V.Its constant 800KHz switching frequency (Sync from 1-1.4MHz)makes noise sensitive circuits stay away from noisy interfering signal, and it can use micro capacitor and inductance.LT3436's High converting efficiency and powered heat dissipation package can provide a big current boost ability in a tight space, suitable for a cramped device.

4. Conclusions

This article designed a high frame rate linear CCD data acquisition system based on USB 2.0 and FPGA. The system uses high performance FPGA as core device, high speed A/D converter is selected for the system. Using VerilogHDL Language for describing the hardware, and using USB interface for transmitting data to meet the requirement of high speed transmission. Experiment shows that system can sample 7500 frames linear CCD image data in a second. Transmission speed of USB2.0 is closed to 200Mbps. It has high anti-interference and high reliability features. It can meet require for high data sampling. It's a high speed and accurate linear CCD data sampling scheme.

References

[1] ZHAO Kai-sheng, LIU Shuang, LONG Zai-chuan, et al.2006, "Scientific Grade CCD Data Acquisition System Based on Embedded Web Server", Journal of Optoelectronics laser, vol.17, No.12, pp 1470 -1473.

[2] ZHEN Mao-fa1,2,FANG Xiao-hong3,LI Xiu-juan, 2007, "Design of the driver circuit based on the high speed CCD data acquisition system", Journal of Anhui University(Natural Sciences), vol.31, No.4, pp 33-35.

[3] Wang Fang, 2006, "Design & Applicational Research on High Speed Signal Acquisition and Processing System", a dissertation submitted in partial satisfaction of the requirements for the Master of Engineering of Northwest Polytechnical University.

[4] Li Yongguan, Xie Xinoping, 1997, "Processing of CCD Output Signal", Journal of Applied Optics, vol.18, No.1, pp 20-23.

[5] HUANG Lei1, Li Zi-tian, MENG Nan, LIU Mei-ying, 2009, "Design for CCD Image Sensor Schedule Generator with High Frame Rate", Chinese Journal of Electron Devices, vol.32, No.2, pp 262-264,268.