Joint Power and Input / Output Line of Mobile Devices

Zhaohe Wang

Software College, University of Science and Technology Liaoning, China

Hhygy453@163.com

Abstract. An electronic device including a host system including a source; and a target system operably coupled to the host system via a combined power I/O line; wherein the target system includes a pass transistor and a switching system cooperative to allow the source to charge a power supply capacitor on the target system via the combined power I/O line in a first mode and alternately charge and discharge the power supply capacitor during a communication via the combined power I/O line in a second mode, wherein the alternately charging and discharging is in synchronization with said communication.

Keywords: combined; power; input/output; line.

1. Introduction

In the field of mobile devices, such as cellular telephone and Blackberries, a small form factor is an increasingly important design consideration. Such devices typically include battery packs having power lines and input/output lines. In some instances, however, the small form factor of battery packs makes it difficult to provide sufficient pins for communicating.

Accordingly, it is known to provide a combined power and input/output pin or pins on an integrated circuit or other device. Such solutions typically include a diode and capacitor or a resistor and capacitor to extract power and store it for the device.

The diode-capacitor solution, however, has proven to be disadvantageous in low voltage systems. More particularly, in such systems, the diode drop may be insurmountable.

The resistor-capacitor solution is disadvantageous owing to baud rate and power consumption contention. That is, low power consumption requires large resistors which require longer on-times and lower baud rates which increase power consumption.

As such, there is a need for a system and method for minimizing the pins for communicating between a power supply and target device. In particular, there is a need for an improved combined power and input/output solution.

2. Joint Power And Input / Output Line

A host system is in communication with a target system. The host system may include a source, transmitter, receiver, and switches, the switches, may be embodied as, for example, switching transistors. The host system couples via a line to the target system. The source may be a current source or a voltage source. Thus, the figures are exemplary only. In operation, the switches, function to switch the current from the source or the transmitter or receiver to drive the host line.

In particular, in a first or power mode, the host system will drive the host line high for a few milliseconds using the source. As seen at time a (FIG. 2), this causes the voltage Vdd to ramp up and gives the target system enough time to be powered by the parasitic diode present in the pass transistor. When sufficient voltage is present on the Vdd power supply capacitor, the pass transistor will become active and the charge rate will increase, as shown at a. The output of OR gate, rectifier drive, follows the host at a. After some time passes, as shown at b, the target device will disconnect the pass transistor, allowing the host system to begin communications without discharging the target power.

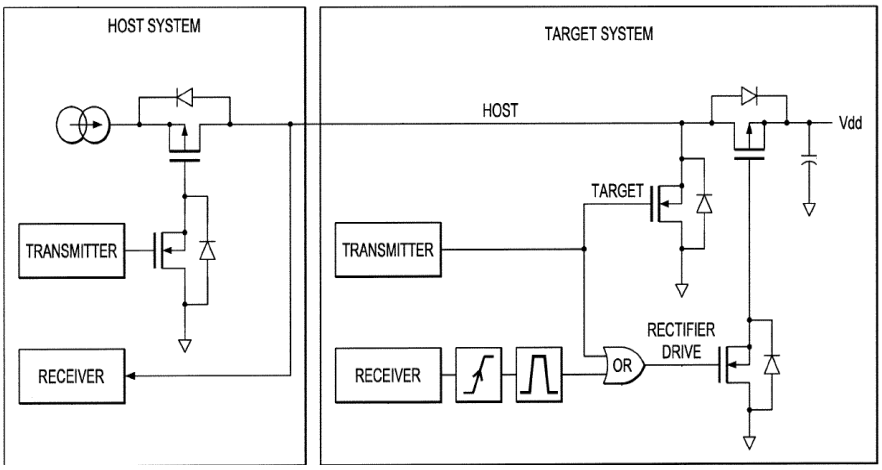

Fig. 1 is a block diagram of a system according

The bit stream from the host on line is shown at b. During this communications mode input phase, the target system will assert the pass transistor for a short period after each rising edge from the host. That is, as shown at a- e, rectifier drive c is high for a brief period, corresponding to the assertion of the pass transistor.

This provides an opportunity for the Vdd capacitor to charge up a little during each data bit, as shown for example, at b. As can be appreciated, the maximum baud rate is dictated by the on period of the pass transistor.

When the host is finished transmitting, it is possible for the target to communicate in an output phase with the host as shown at by pulling the host power line low during each bit, as shown at a. When the target is not pulling the power line low, it can assert the pass transistor for the entire high portion of the data bit, i.e., rectifier drive via transistor. This synchronization is possible because the target knows the entire duration of each data bit.

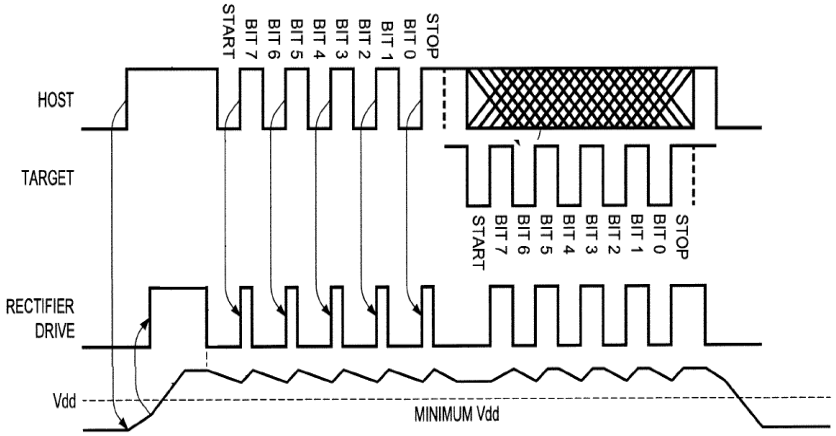

Fig. 2 is a timing diagram illustrating operation of the circuit system

In each case, a host provides power via a pass transistor to charge voltage Vdd. Depending on the embodiment, it can be a switch control, tractate, transistor, or combinations thereof.

3. circuit diagram illustrating

A microcontroller (MCU) acts as the host system and couples via an I/O port to a target system. The target system includes pass transistor and switching system, as well an input system. A power supply capacitor couples to target system and pass transistor via port. I/O line couples I/O port to RX and TX I/O and to the power supply capacitor via pass transistor. The MCU provides host system I/O and a source of current (not shown) to charge the power supply capacitor in a manner similar to that discussed above.

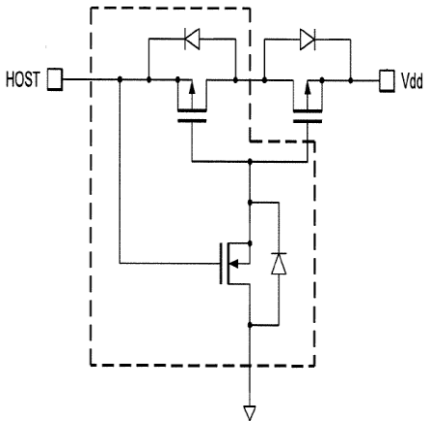

Fig. 3 is a circuit diagram illustrating an embodiment

In operation, the switching system and pass transistor cooperate to allow for I/O operations and power supply operations. Switching system includes AND gate and weak FET and FET. One input of the AND gate is provided by multiplexer of the input system while the other is from a "Strong Drive Enable." The input system includes OR gate which can receive SLEEP and RESET inputs, as well as an input from multiplexer. The SLEEP and RESET inputs allow the capacitor to charge at full speed by enabling transistor during these conditions. When the device wakes, active control of transistor can resume.

4. Conclusion

Although the foregoing specification describes specific embodiments, numerous changes in the details of the embodiments disclosed herein and additional embodiments will be apparent to, and may be made by, persons of ordinary skill in the art having reference to this description. In this context, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of this disclosure.

References

[1] Guo T,Wang H X,Zhang S J.Fluid selection for a low-temperature geothermal organic Rankine cycle by energy and exergy. Asia-Pacific Power and Energy Engineering Conference . 2010

[2] Borsukiewicz-Gozdur A,Nowak W.Maximising the working fluid flow as a way of increasing power output of geothermal power plant. Applied Thermal Engineering . 2007

[3] Heberle F,Brüggemann D.Exergy based fluid selection for a geo- thermal Organic Rankine Cycle for combined heat and power genera- tion. Applied Thermal Engineering . 2010

[4] Iqbal K Z,Fish L W,Starling K E.Isobutane geothermal binary cycle sensitivity analysis. Proceedings of the National Academy of Sciences of the United States of America . 2012

[5] Paloso Jr G,Mohanty B.Cascading vapour aborption cycle with or- ganic rankine cycle for enhancing geothermal power generation. Re- new Energ . 2013

[6] A. Soroureddin,A.S. Mehr,S.M.S. Mahmoudi,M. Yari. Thermodynamic analysis of employing ejector and organic Rankine cycles for GT-MHR waste heat utilization: A comparative study[J]. Energy Conversion and Management . 2013

[7] A. Habibzadeh,M.M. Rashidi,N. Galanis. Analysis of a combined power and ejector-refrigeration cycle using low temperature heat[J]. Energy Conversion and Management . 2013

[8] Xinguo Li,Cuicui Zhao,Xiaochen Hu. Thermodynamic analysis of Organic Rankine Cycle with Ejector[J]. Energy . 2012 (1)

[9] Bertrand F. Tchanche,Gr. Lambrinos,A. Frangoudakis,G. Papadakis. Low-grade heat conversion into power using organic Rankine cycles – A review of various applications[J]. Renewable and Sustainable Energy Reviews . 2011 (8)