Research and Design of Envelope Tracking Amplifier for WLAN 802.11g

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Abstract

A "split-band" envelope tracking amplifier for WLAN 802.11g was proposed. The proposed envelope tracking amplifier consists of a wide-band linear amplifier and a high-efficiency switch amplifier, which can take the advantages of both linear amplifier and switch amplifier. Linear amplifier was a two-stage structure composed of a folded-cascode amplifier stage and a class AB output stage; switch amplifier was based on synchronous Buck DC-DC converter structure, with a driving circuit and an "anti-through" module placed before. The entire envelope tracking amplifier circuit is designed and simulated with JAZZ 0.18μm SiGe BiCMOS process. The simulation results showed that the gain bandwidth of the linear amplifier was about 50.2-MHz, phase margin was 63.9 degree under 5mA bias current. The conduction ratio and switch frequency of the switch amplifier would change dynamic by tracking the non-constant envelope signal.

Keywords

WLAN, envelope tracking amplifier, linear amplifier, switch amplifier.

1. Introduction

In order to transmit more data, WLAN introduces digital modulation technique like OFDM, which can lead the PAR reach 10dB. PA has to work in deeper "back-off" area to meet the stringent linearity requirement with poor efficiency. Therefore, how to design a high efficiency PA for WLAN 802.11g become urgent, especially for battery powered terminals. Envelope tracking has gradually become a promising solution [1].

In this paper, for better integration with HBT PA, proposed envelope tracking amplifier is implemented in SiGe BiCMOS. Part 2 discussed the spectrum character of 802.11g signal and the topology of envelope tracking. Part 3 gives the research and design of the envelope tracking amplifier for WLAN 802.11g. Part 4 presents the experimental measurements and the layout.

2. Principle of Envelope Tracking for WLAN

2.1 The Spectrum character of 802.11g

With the rapid development of digital signal processing, a block diagram of modern envelope tracking system is shown in Fig.1 where the detection of envelope signal and time matching are performed in base-band chip. The envelope tracking amplifier researched in this paper is placed in the collection node of HBT PA with strict isolation. The nonlinear transformation from I(t) and Q(t) to the envelope signal A(t) by DAC will greatly expand the envelope signal bandwidth.

However, from the spectrum of 802.11g shown in fig.2, we can get point that most of the energy is concentrated below 10-MHz [2]. This characteristic of the signal energy implies that a "split-band" envelope amplifier can achieve a high efficiency over a wide bandwidth.

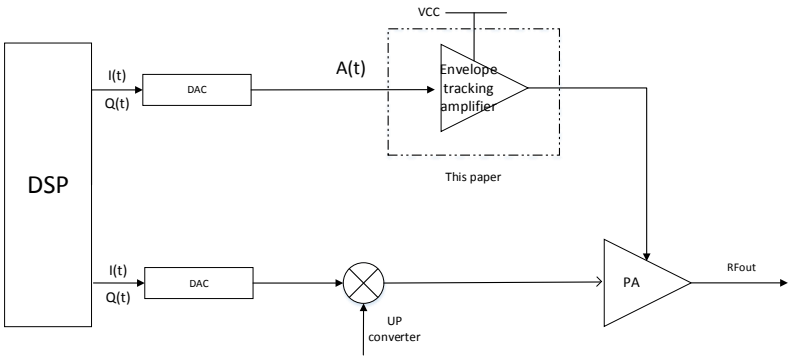

Fig.1 the block diagram of envelope tracking system

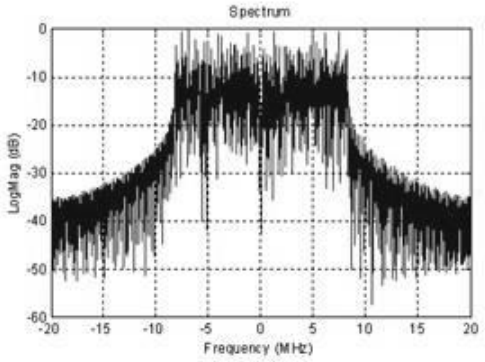

Fig.2 the spectrum of WLAN 802.11g

2.2 The topology of envelope tracking amplifier

The proposed "split-band" envelope amplifier is composed of a wide-band (but rather low-efficiency) linear amplifier and a high-efficiency (narrow-band) switch amplifier, where the overall efficiency is a combination of the two efficiency. The basic structure of the "split-band" envelope tracking amplifier is show in fig.3.

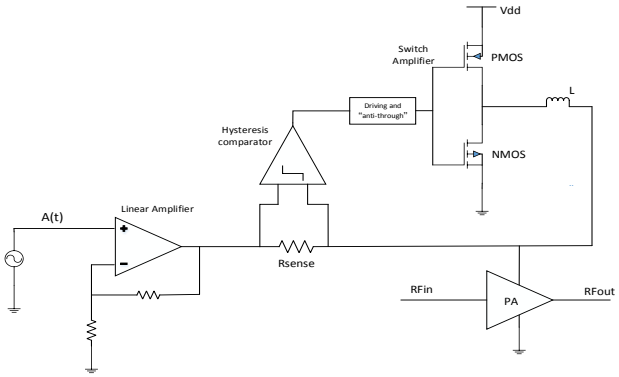

Fig.3 the structure of envelope tracking amplifier

In this case, the switch amplifier operates in parallel with the linear amplifier to get the better performance. The linear amplifier supply the current to the PA when the switch amplifier cannot respond quickly enough, and the switch amplifier operates by sensing the current supplied by the linear amplifier. The optimization result of this analysis is that an optimized switching amplifier operated at a frequency of roughly one-third the envelope signal bandwidth.

3. Research and design of "split-band" envelope tracking amplifier

3.1 The equivalent of PA for envelope tracking amplifier

The overall efficiency η of envelope tracking system show in fig.1 is decided by both the efficiency of PA (η_{PA}) and envelope tracking amplifier (η_{ET}), as the formula (1) shows below:

$$\eta = \eta_{PA} \times \eta_{ET} \tag{1}$$

PA can be equivalent as a load of the envelope tracking amplifier in envelope tracking system to simplify analysis. From research [4], the load impedance R_{load} can be estimated as:

$$R_{load} \approx \frac{\eta_{PA} A_{rms}^2}{P_{out}} \tag{2}$$

Where η_{PA}, P_{out} represent the drain efficiency and the output power of PA, A_{rms} is the root mean square portion of the envelope signal. For example, for a 3.3-V supply voltage and 9-dB PAR signal, the equivalent is approximately 5 Ω for a 40% efficiency PA when the output power is 19-dBm.

In this paper, PA is equivalent as a parallel connection of a 6Ω resistance and a 5pF capacitance.

3.2 Research and design of linear amplifier

Linear amplifier is the most important part of the envelope tracking amplifier, which effects the efficiency and linearity of the envelope tracking amplifier. Beside the traditional require like low output impedance, high loop gain, high gain bandwidth and good linearity, the proposed linear amplifier here also need a high slew rate. For non-constant envelope, highest slew rate is needed in the trough. However, switch amplifier can't provide enough slew rate in the trough, because of the low voltage between the inductance. Research shows, linear amplifier's slew rate need be at least $188 V/\mu s$ under 3V output swing voltage for 802.11g.

In this paper, linear amplifier is a two-stage structure shows in fig.4, first stage is based on a single ended folded-cascode amplifier and output stage is a rail-to-rail class AB structure. The source and sink current of rail-to-rail output stage can be as high as 300mA, in order to reduce the DC power consumption, a low current mirror is used to provide the bias for output stage[3]. The current source is set to 100uA to control the source follower M5/M8, which can make the output M1/M2 operating at a low quiescent current.

Linear amplifier is a two stage structure which means there may be stability problem. C_c, R_c in fig.4 are miller compensation which can provide additional stability for loop. M1/M2 have to bear at least 250mA current which mean their size need to reach a certain size. In this paper, M1 is $3cm \times 0.2\,\mu m$, M2 is $9\,mm \times 0.2\,\mu m$. The approximate input capacitance of output stage is about 25pF, in order to reach a slew rate like $188 V/\mu s$, the bias current I_{bias} of linear amplifier can be estimated as:

$$I_{bias} \cong SR \times C_{in} = (188V/\mu s) \times (25pF) \approx 5mA \tag{3}$$

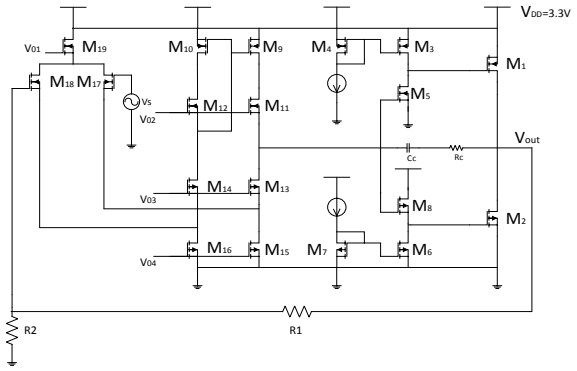

Fig.4 the schematic diagram of two-stage linear amplifier

3.3 Research and design of current feedback control stage

In order to make linear amplifier and switch amplifier work together, a current feedback control stage is needed. As shown in fig.3, the current feedback control stage includes a hysteresis comparator and a detection resistor R_{sense}. In order to reduce the power consumption on the detection part, choose the value of detection resistance much less than that of the load impedance. In this paper, we choose the value equal 0.5Ω. Hysteresis comparator is the comparator with hysteresis width [4] as shown in fig.5.

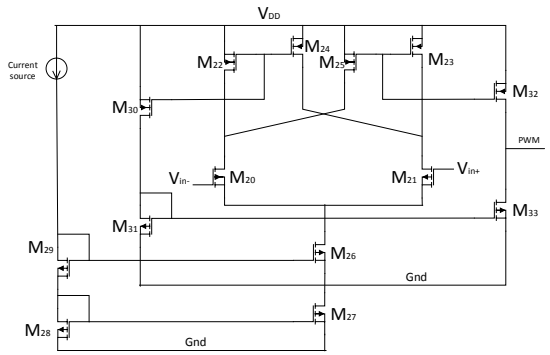

Fig.5 the schematic diagram of hysteresis comparator

Hysteresis comparator is used to eliminate the ripple voltage generated by the switch amplifier due to the switching on and off of the buck DC-DC. The narrower hysteresis width, the better elimination effect of the output ripple voltage. However, the narrower hysteresis width corresponding to higher average switching frequency, which leads to the increase loss of the switch amplifier, then reduce the switching efficiency. Hysteresis width here is a trade-off between the output ripple and the switching efficiency. In this paper, a 12mV hysteresis width is selected.

3.4 Research and design of switch amplifier

As shown in fig.3, switch amplifier is composed of a synchronous buck DC-DC convert [5] with a drive/ "anti-through" stage and an off-chip inductor L. For a low frequency, small amplitude envelope signal, the average switching frequency is about [6]:

$$f_{sw} \approx \frac{R_{\text{sense}}}{L}\frac{A_{DC}}{2h}\left(1-\frac{A_{rms}}{V_{DD}}\right) \tag{4}$$

Among them, A is the envelope signal, including the DC part A_{DC} and the root mean square part A_{rms}, L is the inductance in the switch amplifier, h is the hysteresis width of the current feedback control stage.

In the case of the envelope modulation current slew rate is less than V_{cc}/L, the vast majority of the load current is provided by the inductor (switch amplifier). When the average slew rate of the load current exceeds the average slew rate provided by the switch amplifier, the switching frequency is equal to the envelope frequency, and linear amplifier provides partial load current as source current.

From (4), we know the average switching frequency is connected to the value of inductance. If L is too small, the average switching frequency will be too large leads to large switching loss. If L is too large, the advantage of high efficiency switch amplifier for low frequency can't be fully utilized. In this paper, an off-chip inductor with a value of 2uH is presented.

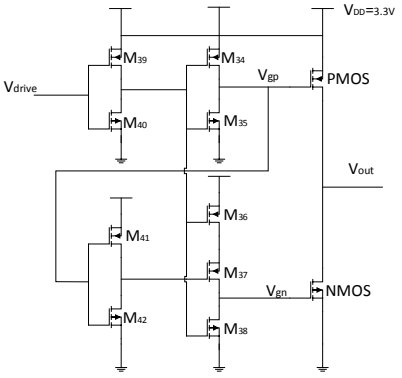

Fig.6 drive and "anti-through" module before DC-DC

Switch amplifier has to deliver large load current up to 450mA, the size of PMOS and NMOS in fig.3 are $8cm \times 0.4\mu m$ and $2cm \times 0.4\mu m$. Large MOS transistor has large gate-source capacitance. In order to drive the buck DC-DC without loss the output slew rate, a drive buffer include M39/M40 and M34/M35 is placed before buck DC-DC [7]. The size of PMOS is much larger than NMOS which

introduce the possibility of shoot through current, so an "anti-through" module include an NAND (M36/M37/M38) and an inverter(M41/M42) is placed before NMOS. The drive/ "anti-through" module is shown in fig.6.

4. Layout and simulation of "split-band" envelope tracking amplifier

The proposed "split-band" envelope tracking amplifier is designed by JAZZ 0.18 μm SiGe BiCMOS process, which can integrate with HBT PA easily. The layout is shown in fig.7, has a size of 600 $\mu m \times 600$ μm.

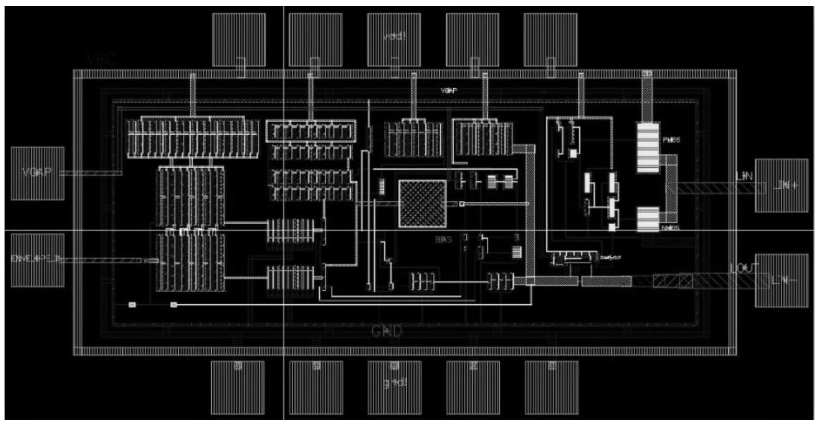

Fig.7 the layout of the envelope tracking amplifier

For 10MHz WLAN 802.11g signal, a unit gain bandwidth of linear amplifier should be at least 30MHz to have a better tracking. In our design, in close loop, linear amplifier has a unit gain bandwidth 50.2MHz, and phase margin is 63.9 degree, which mean the two stage linear amplifier is stable.

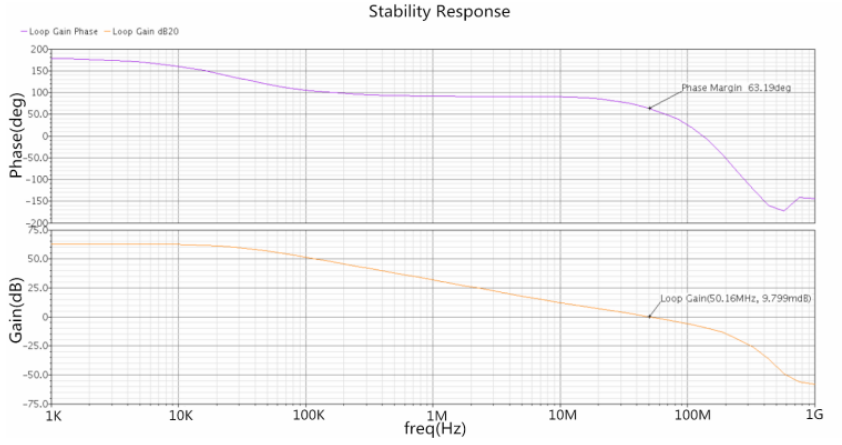

Fig.8 when loop gain is 0dB, phase margin is 63.9 degree

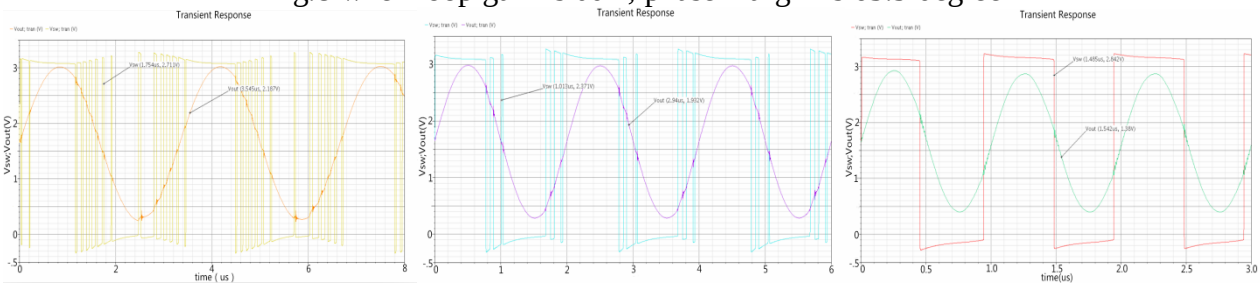

Fig.9 (a) (b) (c) the conduction ratio and switch frequency of the switch amplifier change dynamically by tracking the change of envelope signal

From fig.9(a) (b), when the bandwidth of envelope signal is very low(low frequency), as the amplitude change from trough to peak gradually, the switch conduction radio is also increase gradually, and the conduction radio reach the peak when close the peak of the envelope signal. Compare fig.9 (a) (b), with the increase of bandwidth of signal, the switch conduction decrease from

59.2% to 52.1%. In fig.9, the minimum value of the switch voltage is -0.3V instead of ideal 0V, which is caused by the non-zero conduction voltage drop of NMOS in buck DC-DC.

Compare fig.9(b)(c), when the bandwidth of envelope signal continue increasing, switch conduction decrease slowly and maintained at about 50%, and the switching frequency equal to the bandwidth of envelope signal. This shows that after the efficiency processing of low frequency part of envelope signal, the switching frequency don't goes more higher than the bandwidth of envelope signal which is conductive to reduce power consumption caused by switch amplifier and ensure high efficiency.

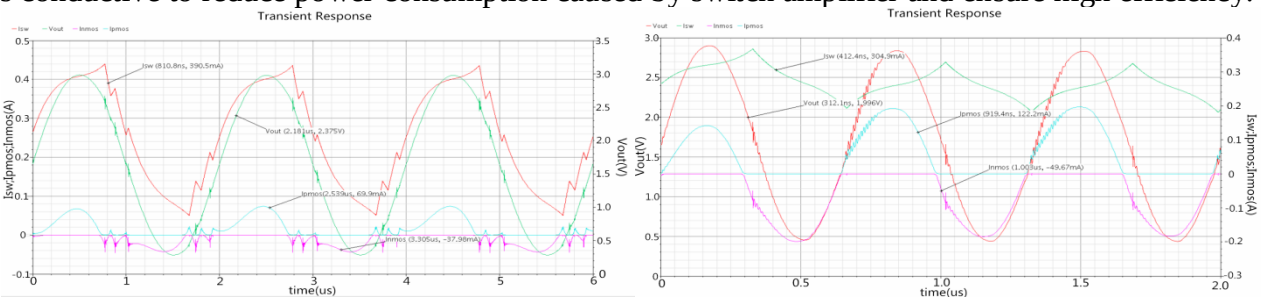

Fig.10 (a) (b) switch and linear current changing with the envelope signal

As shown in fig.10 (a), when the bandwidth of envelope signal is low (low frequency), the load current is mostly supplied by switch amplifier (about 87%). Compare fig.10 (a) (b), as the bandwidth change from 3MHz to 9MHz, linear current in the load current increasing gradually from 13% to 46%. When at the peak, linear provide maximum source current (225mA, fig.10 (b)); when at the trough, linear provide maximum sink current (210mA, fig.10 (b)) and the largest slew rate.

5. Conclusion

According to the spectrum character of WLAN 802.11g that most signal power concentrated in low frequency, a "split-band" envelope tracking amplifier used in envelope tracking system is presented in this paper. Simulation results show that this envelope tracking amplifier can track the expanded envelope of 802.11g perfect and stable. The "split-band" envelope tracking amplifier can track the instantaneous amplitude and bandwidth change of the envelope signal, and change the switching frequency, linear current, switch current dynamically. Actually, besides 802.11g, this envelope tracking amplifier can be used for 5MHz W-CDMA, 8.75MHz WiMAX, even 10MHz LTE.

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