

Fault injection technology in Testability Verification experiment

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Abstract

Fault injection is the key technology in equipment testability verification. With the degree of development of modern equipment, the testability needs to further improve the level, fault injection technology needs further development. Comparative analysis of the common fault injection method, different fault injection methods are classified, the fault injection technique proposed future development prospects, provide technical support and equipment for the verification test work.

Keywords

Testability; Testability Verification; fault injection; external bus.

1. Testability and Testability Verification

Testability refers to the products can be promptly and accurately determine its status (can work, can not work or performance degradation) and isolate one design characteristic of internal faults. With the development of bus technology and other high-tech, equipment complexity, more integrated, testability direct impact on the level of maintenance support capability to play and combat effectiveness of equipment.

The United States and other developed countries deeper research on the issue of weapons testing, and now it has been widely used in aerospace, marine, missiles, armored vehicles, ground complex system. Our test-related technology started late, until the 20th century until the late 1990s in "GJB2547A-1995" defined the general requirements Equipment test work, and because our test validation Assessment System is not perfect, the lack of related hardware and software as a technical support only from abroad means and methods of test, spend a lot of money to buy the test design and verification tools, which for technical research and testing of very unfavorable.

Testability verification experiment is generally in the development stage and setting stages. In the product development process, in order to confirm whether the product is developed to meet the design requirements of the test, to identify design flaws, requiring multiple test validation trials; for what has been established and equipped troops, while it's unable to measure the design for testability level, in order to obtain the test-related data, found that the test design flaws, suggest improvements to improved equipment and more to meet the requirements of design for testability, testability achieve growth, we also need to be tested styling equipment verification test.

2. Key Technology - fault injection technology

We can verify that a fault is detected by BIT by injecting fault into UUT, by comparing fault sample with the results of fault detection, we can reach the point whether the design for testability level reach the target product. Testability verification test usually need to inject a lot of fault samples, so for different unit under test requires a different fault injection method.

2.1 Fault injection methods and classification

Fault injection technique is a key technology, targeted at different levels, different types of units, fault injection method that adapted is different. Fault injection method at this stage can be divided into different types according to different criteria. For example, according to the type of fault classification, it can be divided into hardware and software fault injection; according to the level of abstraction of Fault System, it can be divided into transistor switch level, gate level, chip-level, system-level, application level and so on; according to the implementation of the fault injection, it can be divided

into analog implementation of fault injection method based on fault injection method and physical implementation based on categories. The main example is MADE, TEAMS, or other hardware supporting software to establish a simulation model based on the unit under test simulated fault injection method achieved through the use of software on your computer, and optimize the selected test points for fault injection or insertion failures in the internal model unit achieve fault injection. This method is relatively low cost, flexible test points selected, but the fault model workload, can not fully simulate the actual test unit, so that the credibility is not high in the field of engineering, test verification test as often assisted verification means. This paper will introduce that based on fault injection method for physical implementation, this method is actually injected into the presence of a fault, it is divided into manual and automated fault injection method fault injection method.

Manual operation is more intuitive that commonly used in the testing of the authentication information is not high degree of unit under test, of which the means comprises pin short-circuit components, remove components from the socket replaced with a normal fault Component like, for example, a plug-in fault injection method has some disadvantages, such as easy to damage the unit under test, a small range of applications, maintenance cost, etc., but in guaranteed not to cause irreversible damage to the unit under test, plug-in method convenient, fast, targeted and so on. For example, cable unplug / plug operation, power off / are fault injection method of operating and other connections, which is a more intuitive approach. Fault injection means more automation, but also in recent years in terms of widely used test validation methods, mainly divided into hardware-based fault injection method and the method based on fault injection software. The following will be automated fault injection method detailed classification comparison.

2.2 Hardware-based fault injection method

Bus based fault injection

Current information is a higher degree of integration of equipment commonly used by the bus structure, the bus based on fault injection method is one of the widely used current methods. Bus is a collection of interconnected signal standard is a standard highways. Under normal circumstances, the use of the bus by the scope and functions of the following categories.

- (1) On-chip bus: chip message passing, for example: data bus.
- (2) Chip bus: refers to the standard chip bus interface provides information between chips or devices, such as microprocessors pins constitute the microprocessor address, data and status buses. For chip bus with control functions, since most of the system bus in the microprocessor chip bus is the same, so the bus is a microprocessor fault injection prime location pins.
- (3) System bus: refers to the system bus between the modules of the system access information, such as the system address, data, control and status bus.
- (4) External bus: external bus refers to the communication bus systems, including serial and parallel buses. Based on the external bus fault injection usually under excitation signal it is applied to simulate the fault and then poured into the external interface of the unit under test. Its essence is to enter the desired address fault signal, replacing the normal signal and then output to the next-stage circuit. Fault injection conditions determine the injection time and injection times.

Overall, the external bus fault injects in two ways. One is the excitation signal simulation before sending the excitation signal failure. Such as: the need to validate a master device receives the slave device returns the self-test handling of exceptions. By this time the slave device simulation will be used, when the master device sends a self-test command, returned by the slave device self-test abnormal results, observe handling the case after the master device receives feedback on the master device for evaluation. The advantage of this approach is that the injection of low cost, less demanding equipment, most of the simulation board can complete the task. The disadvantage is that the excitation signal generating time-consuming, difficult to produce a complete excitation signal, and can only communicate fault injection. The other is in series between the actual test equipment and the tested one. To verify that a master device receives the slave device returns the self-test handling of

exceptions. At this time turn off the communication between master and slave devices external bus, the slave device returns the signal into fault injection device, the injection device fault signal output to the master device. This time in the real-time monitoring equipment fault injection signal on the bus, when the slave device generates a self-test signal is input to the fault injection device, and then fault injection device will analysis the signal, if the returned signal is a self-test information, the self-test information replace abnormal signal, and then outputs the abnormal signal to the master, then the master device after receiving the feedback signal will be evaluated. The advantage of this method is that the fault injection failure mode coverage is high, and because the test equipment and the device under test is an actual device, high reliability, good stability, while achieving the bus physical layer, protocol layer and electrical layer fault injection. For the physical layer, the electrical layer, protocol layers, it has different failure modes and fault injection methods, e.g., the physical layer may realize short-circuit, open circuit failure, protocol layers can delay the signal output fault. Currently directed to 1553B, CAN, RS232 and other bus has faced to the market.

Probe fault injection

Directed to component level of the unit under test, testers can complete the component pin connection at the unit under test and inject fault through the probe, it changes the electrical device pins or changed between components connection, it will pull down voltage of chip or pin, or add resistors, capacitors and the like to change the physical connection. Its disadvantage is the need to destroy the circuit board anti-skinning and wire insulation, because of the actual and complex working conditions with tight packaging and other products, so there will not reach probes and so on. Common fault injection method based on the probe includes a rear drive, switch cascade voltage summing fault injection method.

Cable fault injection

Between the plurality of circuit boards in the unit under test or at connection line of multiple devices, you can use switches fault injection method, which through the fault selecting circuit selects the fault path, the use of analog circuit simulation signal malfunction of the circuit. It may be connected to line damage and reconstruction, but its relatively low cost, the basic body of the unit under test does not cause irreversible damage.

Adapter plate fault injection

This method requires a special adapter plate, which is connected to the intra-replaceable units of several boards, simulation produced within the field replaceable unit internal fault or external physical layer fault. This method can also be referred to the backplane bus fault injection, which by changing the physical connection of the circuit board, signals, data, etc. to achieve fault simulation. With respect to the external bus injection method, its scope is non-standard PCI bus and backplane bus.

Summary

The above description of the hardware-based fault injection method is relatively mature, but the more obvious drawbacks, as the equipment of high complexity, the package is good, the more the degree of information-intensive, thereby causing difficulty of injection, high expenses, destructive and other issues affecting the overall testability verification process, it makes people do not believe in the Party to verify the results, it is difficult to give high reliability of test validation and assessment findings, it is necessary to look for alternative methods, combined with simulated fault injection methods, suitable for different devices using fault injection means.

2.3 Software-based fault injection method

The method is mainly for generation software level fault mode, and then injected into the system software to go, then the measured object functions for fault detection. This fault injection method widely used in the PC, because the design will be modern equipment in the main control system, or MCU control engineering or computer control software, so for software fault injection and diverse ways. Currently fault injection software is divided into static and dynamic injection in two ways.

Static fault injection method

The method is the way that before running the software, injecting fault by directly modifying the source code. For example: the product functionality has received instruction exception handling, processing behavior in order to receive commands from the software trigger abnormal, through failure analysis, failure mode will be located to the software level, can be found to produce instruction receives a variable to a specific value exception error. At this point you can modify the source code, this variable is assigned to a specific constant value, compiled, downloaded to the target system when performing this function, receiving instruction triggers exception handling behavior, the behavior observed by subsequent processing of products, to evaluate the product. The advantage of this approach is that the implantation condition of the fault injection is simple, just need to modify the source code section, compile to complete fault injection, this costs lower, high fault coverage. The disadvantage is the lack of real-time, and needs to frequently modify the source code for different parts, that increases the difficulty of fault injection control.

Dynamic fault injection method

The method refers to inject faults dynamically as the software running. The lightweight kernel will run in the target system responsibly for fault injection. Originally applications interact with the target system, after running into a lightweight kernel applications interact with the kernel, the kernel and then interact with the target system, this time by controlling this lightweight executable kernel fault injection. Advantages of dynamic fault injection is that it has a fault injection management capabilities for fault injection tube monitor, fault injection and develop strategies automatically executed after the trigger, this method with respect to the static fault injection is more suitable for the actual study. However, its disadvantage is that the target system has more stringent requirements, and higher costs.

3. Fault Injection Technology

The purpose is to generate fault injection fault, then test the function of equipment and access to data. In the design and demonstration stage, prototype verification stage and the use stage of equipment development requires fault injection, the following targeted at different stages elaborate application fault injection technique:

- (1) In the design and demonstration stage, fault injection technique is mainly used to generate, analyze design flaws, thereby improving equipment designs. Since at this stage there is no test prototype, so we use simulation-based fault injection technique for product demonstration.
- (2) In the prototype stage, fault injection is mainly used to analyze the performance of the test equipment related hardware and software, etc. are whether defective or not, then the fault may be injected directly to the target cell. As the prototype stage equipment had actually exists, it can be based on a physical fault injection technology including software, hardware fault injection techniques to test the prototype validation.
- (3) In the use stage, fault injection techniques can analyze equipment failure has occurred or will occur. After producing the fault, you can analyze the type of fault, fault impact and can be combined using the PHM failure prediction technology to provide data support for improved or new models of equipment development. Since the use of stage equipment has been finalized, the package of opportunity to reduce the lead to fault injection, now we use bus-based fault injection technique more for testing verification and analysis.

Comprehensive testing of domestic equipment construction as a whole, the fault injection technique is mainly used in prototype stage. This is because in the equipment design validation stage, it is difficult to obtain a sufficient argument to support the establishment, and the long cycle modeling, heavy workload and the complexity of the case; while in the using stage, since the equipment early in the design verification test did not fully consider the relevant factors, the encapsulation of equipment leads that we can not inject fault, so the fault injection technique is more difficult to study in this stage.

4. Fault injection technology foresight

With the improvement of integration and encapsulation, the equipment will continue to develop along the information, intelligence development. In this trend background, the test process need to study current developments in equipment, fault injection technology research should also tend to be more intelligent. Extensive theoretical research tool fault injection should be applied in practice, and explore the hardware and software methods to study the portable, intelligent fault injection terminal, software development should learn from foreign advanced software such as basic TEAMS, MADe and so on, and gradually develop the domestic universal supporting software. Fault injection technique should be combined with fault sample selection, fault sample dispensing failure of new technologies to form a system failure to apply the test of the study.

References

- [1] HUANG Yongfei, PENG Xinjie. A Method of Fault Injection in Normal Circuit[J]. AERO WEAPONRY, 2007, 4(2).
- [2] SUN Junchao, WANG Jianying, YANG Xiaozong. The Present Situation for Research of Fault Injection Methodology and Tools[J]. Journal of Astronautics, 2001(1):99- 104.
- [3] YANG Dongjian, WANG Hong, LIU Jinfu. Design- for- Testability and Validation Technology of Aeronautic Equipment[J]. Measurement & Control Technology, 2006, 25(10):1-5.
- [4] Wulf N, Cieslewski G, Gordon-Ross A, et al. SCIPS: An emulation methodology for fault injection in processor caches[C]. Aerospace Conference, 2011:1-9.
- [5] Jeitler M, Delvai M, Reichor S. FuSE-a hardware accelerated HDL fault injection tool[C]. 5th Southern Conference on Programmable Logic, 2009:89-94.