Research on Exact Integral Double Forward Converter by Nonlinear Control

Qiangnan Du, Zhanping Li

College of Electrical Information Engineering, Northeast Petroleum University, Daqing, 163318, China

Abstract

The PWM switch converter essentially belongs to the nonlinear control system. Based on the PID control converter in the system dynamic response, robustness is very difficult to obtain satisfaction the control effect. The comprehensive survey domestic and foreign proposed in recent years several kind of non-linear controls strategy, the one-cycle control has the big superiority in the control effect and the project realization aspect, and has been applied in some PWM converter. The one-cycle control through uses a non-linear integrator, forces the switch converter medium in each switch cycle in the datum, crossed the converter output stage, thus reduces the systems control step number, causes the system to suppress inputs the dynamic response which the power source disturbs to enhance greatly. The one-cycle control shortcoming mainly is to the switch error adjustment ability limited, the system existence static error, at the same time the system load dynamic speed of response is slow.

Keywords

Nonlinear Control, The Exact Cycle Integral Function Control, Simulation.

1. Introduction

Owing to the superiority of low voltage stress of the switch tube, the input and output isolation, and can realize multiple output voltage and so on, Double Forward Converter is a topology used frequently in switch power converters[1]. Control method often adopts voltage single loop or voltage-current double closed loop linear feedback control theory. Due to the switching power supply is a very strong nonlinear system. Application of linear feedback control systems in switching power supply controlling can not satisfy the control effect of system dynamic response, robustness and steady-state error. Therefore, in recent years, many domestic and foreign scholars have made a deep research on the control strategy of switching power supply, and have proposed kinds of non-linear controls strategy such as sliding mode variable control[2], fuzzy control[3], One-Cycle Control[4] and so on, which have made some progress.

2. Fundamental principle of exact cycle integral function control

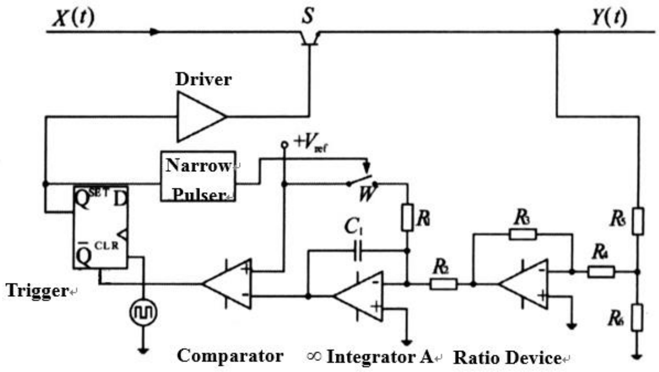

Figure 1 Switch regulator of exact cycle integral function control

The working principle of exact cycle integral function control switch regulator is shown in figure 1. The system consists of an operational amplifier, nonlinear integrator, comparator, divider, narrow pulse generator and reset switch. The working waveform of each point of the controller is shown in figure 2. At the time of the arrival of the pulse rising edge of the clock, The flip-flop is set (Q=1), the drive switch S is turned on, the switch output $y(t)=x(t)$. After sampling circuit and operational amplifier, the signal $y(t)$ is changed into V_p, And connected to the integrator to output integration of signal $y(t)$. The output of the integrator, V_{int}, began to grow linearly in the forward direction from initial value of V_{r1}.When V_{int} reaches control reference value V_{ref}, the comparator output flips, the D flip flop reset (Q=0), Switch S off. Off signal generates a signal By means of a narrow pulse generator at the same time, turning off the reset switch W and achieving reverse linear reset of integrator. It is worth noting that the integrator output in this process is not reset to zero (integrator of one cycle control in each period will be completely reset), but according to the size of the output $y(t)$ and the unique switching time of the controlled switch S itself, automatically reset to an initial value (for example V_{r1}). When the next clock cycle arrives, integrator restarts next cycle of the integral work from the reset value of previous cycle, and again and again[9-11].

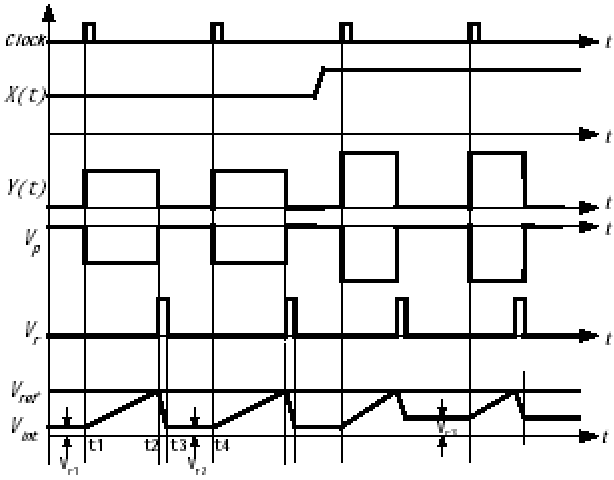

Figure 2 Work waveform of exact cycle integral function control

3. Features and improvements of exact cycle integral function control

In exact cycle integral function controller, the integrator of core part does not adopt the parallel switch reset mode (Single cycle control using parallel mode) but introduces a narrow pulse linear backward reset. The advantage of this reset method is that: The output signal of controlled variables works as input of integrator in the whole closed-loop control process, therefore, in each switching cycle, the output of the integrator can not be completely reset to zero but automatically reset to an initial value according to the actual physical characteristics of the controlled switch variable. The signal amplitude of the controlled switch variable is higher, the initial value of integrator after reset is greater, so the time of the integrator output reach to control reference V_{ref} in the next cycle is correspondingly shorter[5-7]. The difference between integrator initial values of adjacent switch cycle is proportional to the switching error:

$$\Delta V_i = V_{i1} - V_{i2} = k \cdot \int_0^{T_{reset}} \left[y_1(t) - y_2(t) \right] \cdot \mathrm{d}t \tag{1}$$

It should be noted that there is also another problem after exact cycle integral function control solving the problem of switching error in single cycle control, that is the integrator will cause saturation and system oscillation while the hopping of converters load lead inductor current to change from continuous mode (CCM) to discontinuous mode(DCM). This problem also exists in the single cycle control. After careful analysis, it is inductor current is zero that lead integrator saturation. Diode voltage equals to the output voltage V_0, and this time V_0 has a serious overshoot due to load disturbance, the peak value is greater than the steady state value of output voltage. Therefore, before integrator starting from the initial value to the next clock to the arrival of the clock, it will achieve control benchmark and flip the comparator. And because the previous flip flop is in the off state, the comparator flips without changing the state of the trigger. Thus it is impossible to generate a reset signal. So the integrator will continue to integral and eventually lead to saturation.

After the double feed-forward compensation network, the formula (4) is changed into:

$$\int_0^{T_s} \frac{k_1 \cdot k_2}{R_2 C_1} \cdot V_D \cdot dt + \int_0^{T_s} i_c(t) \cdot dt + \int_0^{T_s} V_0(t) \cdot dt = \int_0^{T_{ret}} \frac{1}{R_1 C_1} \cdot V_{ref}(t) \cdot dt \qquad (2)$$

In the above formula, when system in steady state, detection current of the filter capacitor is a periodic change of the symmetric time axis, so its integral in a switching cycle is zero. The output voltage in a switching cycle is zero. That is:

$$\int_0^{T_s} i_c(t) \cdot dt = 0 \qquad (3)$$

$$\int_0^{T_s} V_0(t) \cdot dt = 0 \qquad (4)$$

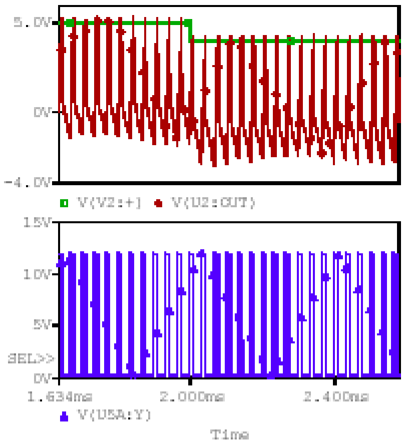

Figure 3 Control reference, integrator output control and driving waveform

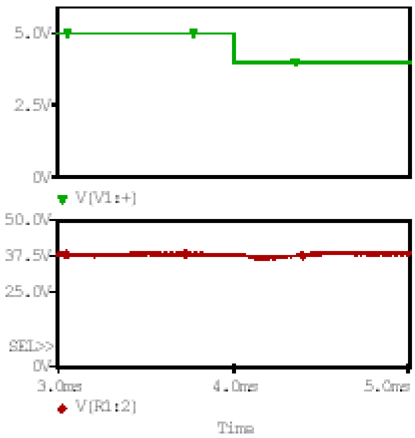

Figure 4 control reference and simulation waveforms of output voltage

At present, the output element of the PWM switch converter adopts low pass filtering link consist of inductance capacitance, the time constant of LC filter is usually very large, so the filter is actually turned into a large inertia link. But the ability to restrain the load disturbance is not ideal, and other improvement measures must be studied. In the automatic control system, in order to eliminate the influence of the disturbance to the output, add feed-forward control which is more timely than feed-back control and will not be affected by the delay of the system. Feed-forward control is widely used in the system requires the output to be able to follow the input quickly. In terms of switching converters, load current or filter capacitance current is an external disturbance signal. When the load of converter suddenly increase or decrease, the DC output voltage will be affected firstly deviating from the set value. Then system enters steady state again by adjusting voltage close loop regulator. But due to the effect of output low pass filtering time constant, the regulating function of the voltage regulator is slow. So introduce reasonable designed load current feed forward control in the PWM switch converter will significantly improve the load dynamic response of converter.

4. Double transistor forward converters of exact cycle integral function control with feed-forward compensation

In order to verify the correctness of double transistor forward converters of exact cycle integral function control with feed-forward compensation. Circuit simulation is carried out by using circuit simulation software PSPICE. Circuit parameters are as follows: Input voltage is 400V, switching frequency is 30KHz, output filter inductor is 250 uH , output filter capacitor is 50 uf , the load is 5Ω.

(1)Tracking control benchmark simulation: Figure 4 is the control reference, the integrator output control and driving waveform. Figure 5 is the control reference and simulation waveforms of output voltage. When the input power and output load remain unchanged, and the control reference jumps from 5V to 4V in 2ms, because the output voltage is not changed, the voltage V_D outputted through the secondary side of the main transformer to the rectifier diode is not changed, so does the input value of the integrator after sampling feedback and the slope of integrator positive linear integral. Just at the time of the jump, and finally stabilized at around 37.5V. It shows that the system has a good performance to follow the change of the control reference.

5. Conclusion

Research team proposed new strategy of exact cycle integral function, summarized its characteristics and proposed modified double feed-forward exact cycle integral function control strategy. Adopt exact cycle integral function control with feed-forward compensation in double transistor forward converters. Analysis and verify the disturbance of suppress power supply, suppress control reference and suppress load of this control strategy through the simulation waveform. It can concluded from theoretical analysis and simulation results that the exact cycle integral function control with feed-forward compensation basically achieves the optimal control, the dynamic response is fast and can achieve no errors at stable state.

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