Characterization of Single-Photon Avalanche Diode in 0.18μm Standard CMOS Process

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Abstract

This paper introduced a silicon single photon avalanche diodes(SPAD) in 0.18um standard CMOS process. The basic structure of the proposed SPAD is p+/n-well/DNW/p-sub. The design and simulation of structural parameters and process parameter that lead to such low breakdown voltage, high photon detection efficiency(PDE), low dark count rate(DCR) are reported and analyzed. The device's key parameters are extracted from Silvaco simulations results. The active junction of the suggested SPAD diameter is 20um. Edge breakdown is prematured by utilizing a p-sub virtual guard ring(GR). The simulation results show that: with the p-sub GR, the SPAD unit responsivity as high as 0.38A/W, the breakdown voltage is 13V, the quantum efficiency(QE) is 78%, the PDE is 47% and 51% when the excess bias is 1V and 2V, respectively. The improved 3dB bandwidth is 2GHz and the DCR is 6.2kHz when bias voltage is 14V. The key features of simulation that give physical insight on how to design low breakdown voltage, high photon detection efficiency and low noise SPAD.

Keywords

Single Photon Avalanche Diodes(SPAD); Avalanche Breakdown; 0.18um Standard CMOS Process; 3db Bandwidth; Photon Detection Efficiency(PDE); Dark Count Rate(DCR).

1. Introduction

Single photon avalanche diodes owing to its ultimate optical sensitivity and high internal gain have become a process of choice in many applications. For instance, they are now used in high speed optical receiver, fluorescence lifetime imaging microscopy, ultraweak chemiluminescence measurements [1-3]. In consideration of the silicon material is cheaper than III-V and Ge material, and more suitable for design the widely applied SPAD. Thus SPAD have been rapidly advanced. More importantly, there are significant efforts devoted from experts and scholars from all over the world to design SPAD in CMOS process. The carries diffusing is so slow that impact the diffusion speed. The way to increase the SPAD response speed is to use double photodiode structure by extending the width of the depletion region suitablely [4]. The double junctions structure, one is p+n-well junction, the other is the deep n-well/p-substrate junction. The general SPAD structure p+/n-well/deep n- well/p-sub is improved its a variety of performances and widely researched for the past few years.

In 2010, Emmanuel R. Moutaye et al [5]. Comparison p+n APD structure and n+p APD structure in standard 0.35um CMOS process. Finding that the p+n APD presented the best responsivity with a peak around 550nm, and the n+p APD presents a peak of responsivity around 450nm. Because the previous one has a deeper depletion region than the latter one. In 2013, Mohamed Atef et al [6], reported a silicon avalanche double photodiode (p+/n-well/p-substrate) fabricated in 40nm standard CMOS process. At 520nm, the avalanche double photodiode responsivity of 2.04A/W and 3dB bandwidth of 1.4GHz are achieved, the value is much bigger than the traditional APD. A SPAD is realized by p+/n-well junction in 130nm COMS deep submicrometer process in 2011 [7]. The SPAD operating in geiger mode for a particular purpose. The avalanche voltage is 17.9V, the peak PDE up to 33% at 1.2V excess bias at 450nm. A CMOS SPAD is realized by p+/n-well/deep n-well/p-sub

double junctions structure in a low voltage 180nm CMOS process.. the max PDE is 48% at an excess bias of 3.3V in 430nm when the breakdown voltage is 21.4V in 12um diameter, Tomer Leitner [8] reported in 2013.

In this paper, we study single photon avalanche diodes based on 0.18um standard CMOS process. This paper is organized as follows: Section 2 presents single photon avalanche diodes structure model. Section 3 establishes single photon avalanche diodes photometric characteristics, as well as discusses and compares with others SPAD performances. Finally, Section 4 concludes the paper and points out further work.

2. Device Structure Design

In this paper, the SPAD with a p+/n-well/DNW/p-sub double junctions structure in a standard 0.18um CMOS process is designed. The cathode terminal connection is formed by n-well with n+ contact, down to link deep n-well. The anode is created with the use of p+ layer with p+ contact. The SPAD is operated in the region when the applied reverse bias voltage above the breakdown voltage, a self-sustaining avalanche is established. The SPAD with p-sub GR, as shown in Figure 1, provide a tradeoff between fill factor and large edge electric field and it is a feasible way to validate the efficiency of the applied GRs.

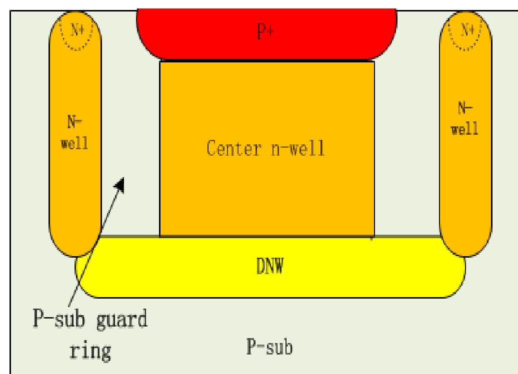

Fig 1. The structure of p-sub GR SPAD.

In fig 1, the n-well is cleaved into two n-wells separated by a small gap (about 1um) constituting the p-sub guard ring, doping concentration is 1e15cm-3. Guard rings premature edge breakdown effect since higher electric field exists at the periphery in SPAD. P+/n-well junction is active area, charge multiplication events will be triggered in this region. This SPAD p+ layer doping concentration is designed at 5e19cm-3 and n-well doping concentration is 1e17cm-3 so that can make sure occur avalanche mechanism smoothly. The deep n-well/p-substrate junction main function is reducing substrate interference so that substrate carries cannot enter into the active region. The designed deep n-well is connected to the n-well contact through the p-well and p-sub guard ring structure. The rest of structure parameters of these SPAD are shown in table 1.

Table 1.P-sub GR SPAD structure parameters

Layer	Doping/cm-3	Depth/um
p+	5×10^{19}	0.8
n-well	5×10^{17}	2
DNW	5×10^{15}	2.3
p-sub GR	1×10^{15}	2
p-sub	1×10^{15}	-

3. Simulation Resoults and Discuss

3.1 IV characteristics

Fig 2 showed the electric field distribution. We find that the max electric field is occur in p+/center n-well junction. The max electric field value is up to 5.7V/cm with p-sub GR SPAD We can use the following formula to calculate the theory value of breakdown voltage.

$$V_B = \frac{1}{2}\delta_m W_D = \frac{\varepsilon_S \delta_m^{\ 2}}{2qN} \tag{1}$$

In the formula, is the max electric field, N is pn junction light doping nocation (this paper is $1\times10^{17}cm^{-3}$), is silicon dielectric constant (about $1.045\times10^{-12}F/m$) The p-sub GR SPAD in theory calculation breakdown voltage are 10.1V.

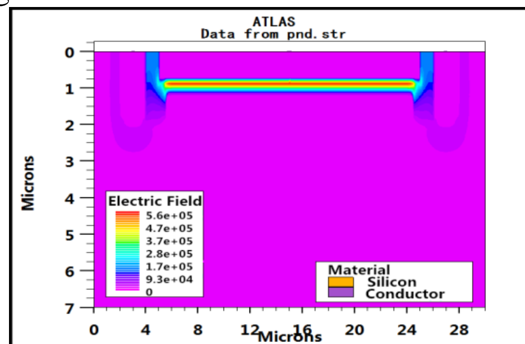

Fig 2. The electric field distribution of p-sub GR SPAD

Fig 3 showed I-V characteristics for different light powers in the SPAD. The light powers are 30mW 3mW 0.3mW. Regular, The light power is bigger the photocurrent in small bias voltage is bigger, but in avalanche region different light powers photocurrent is the same. P-sub GR SPAD breakdown voltage is bigger than the theory breakdown voltage value, because the GR design methodology to avoid edge breakdown thus improve the device withstanding voltage.

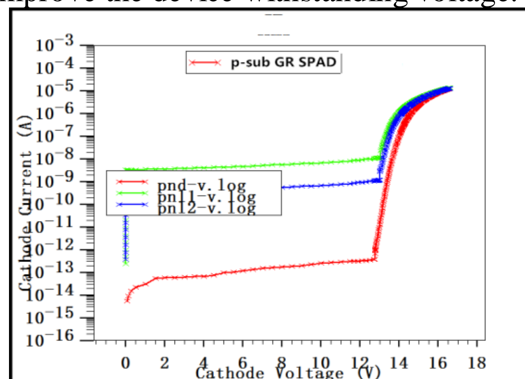

Fig 3. The I-V characteristics of different light powers in p-sub GR SPAD.

3.2 DC responsivity

With p-sub GR SPAD responsivity curves in fig 4 show maxima responsivity are 0.38A/W in 620nm at excess bias 1V. The low responsivity for short wavelengths at low biasing region compared to the larger responsivity around 620nm wavelenth can be explaned by two reasons. First one is the short wavelengths light have strong reflection. Second one is the p+ layer depth is only 0.8um, the short wavelengths partial absorption. 620nm wavelength is strongly absorbed before the multiplication region, and have an electron injection in the multiplication region.

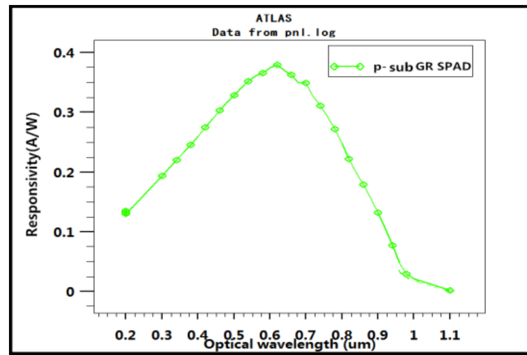

Fig 4. The responsivity of p-sub GR SPAD and p-well GR SPAD.

3.3 Photo detection efficiency

QE is the radio of detect events to incident photons. Using the formula (2) to calculate the QE value

$$R=\frac{I_{\text{ph}}}{P_{\text{opt}}}=\frac{\eta\cdot q}{h\cdot v}=\frac{\eta\lambda_0(\mu\text{m})}{1.24} \quad (2)$$

I_{ph} is photocurrent, P_{opt} is incident light power, h is Planck constant (6.63×10^{-34}J s). Get the QE values are up to 85% with p-sub GR SPAD. Obviously, the QE is higher than Ref [4], because this paper SPAD have deeper active area. In addition, the lower gain of long wavelengths results from the lower ionization coefficient of holes than electrons, so they undergo a reduced gain.

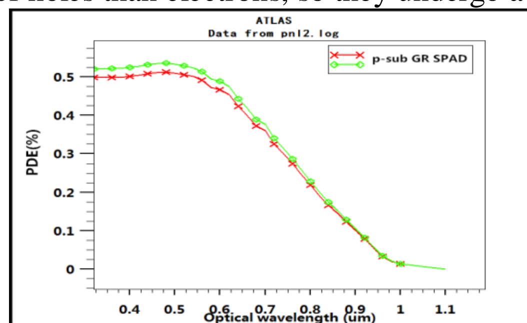

Fig5. The PDE of p-sub GR SPAD at 1V and 2V excess bias voltage.

In fig 5 there is an incident light power 10uW. The maximin PDE up to 51% at 1V excess bias voltage and 53% at 2V excess bias voltage at 480nm wavelength in p-sub GR SPAD.

3.4 Dark count rate

DCR is the rate of events generated while the detector is in complete darkness. Note that this can differ from dark count current, some fraction of which might not generate events; this is the case for dark charge that is not amplified enough to trigger the event discriminating circuitry. Commercially available process and device simulation can be used to accurately predict diode breakdown voltage but cannot directly predict the dark count in SPAD devices. There are two ways of dark current: surface leakage current and bulk leakage current. Bulk leakage current is larger than surface leakage current. Analytical solution exist to calculate dark count and are used to form the basis for the calculation of the minimum theoretical dark count [9].

$$C_{dark}=(I/q)*P_{ai} \quad (3)$$

Where Cdark is dark count rate, q is the electron charge, Pai is the probability that an electron of SPAD bulk leakage current causes an avalanche breakdown. In fig7 we can see the p-sub GR SPAD DCR under different temperature. They are all around kHz. The p-sub GR SPAD DCR is 6.2KHz and the at excess bias 1V at 300k temperature.

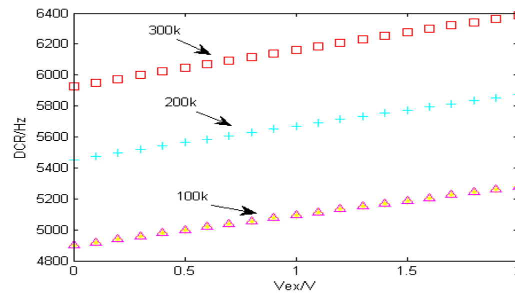

Fig7. The DCR of different temperature in p-sub GR SPAD.

4. Conclusion

With the p-sub GR, p+/n-well/deep n-well/p-substrate structure SPAD, the active area diameter in 20um breakdown voltage is 13V. The highest unit responsivity is 0.38A/W at excess bias 1V. Using the formula calculating the quantum efficiency are 78%, the PDE are 51% at excess bias 1V. The 3dB bandwidth is 2GHz and the DCR is 6.2KHz at excess bias 1V. This work creates potential for eliminating slow photocarries using extra on the deep n-well. The extra bias in the SPAD not only block the hole and collect electrons form the substrate, but also improves the SPAD performances.

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