Design of a Low Noise Amplifier in 0.18μm SiGe BiCMOS Technology

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Abstract

A 60GHz LNA with a three stage single ended is designed in 0.18μm SiGe BiCMOS technology. The LC resonance is used in the inter stage matching to reduce the transmission loss,by adding a parallel capacitor between two poles to reduce the effect of parasitic.From the simulation results,we can draw a conclusion that:S21 and the Noise Figure are achieved 21.6dB and 5.5dB respectively, in operating frequency of 60 GHz, both input and output return losses S11 and S22 are below -10dB from 55GHz to 65 GHz,the pow consumption only 12.8mw with supply voltage of 3.3V.

Keywords

0.18μm SiGe BiCMOS, Low Power Consumption, 60GHz LNA.

1. Introduction

A receiver in mm-wave frequency, low noise amplifier (LNA) is an important part, it has a decisive influence on the sensitivity of the receiver [1]. The general requirements of low noise amplifier, not only have a very low Noise Figure (NF), but also to provide high enough gain to suppress the noise of the rear stage, the input impedance should be matched to 50Ω, also The linearity of the low noise amplifier need to meet certain requirements. In a variety of low noise amplifier in BiCMOS technology, cascode structure is widely used because the structure can well meet requirements in most cases.

The widespread use of mobile devices proposed more stringent restrictions on the power circuit, low power design has become a trend. For example,low noise amplifier, mixer, power filter and commercial GPS were integrated in a receiver chip,the power is generally no more than 40 mW. In low power constraints, design low noise amplifier with method of the traditional cascode structure has faced some difficulties, need to put forward a new method to solve the problem.

On power constraints, Reference [2] introduces a noise optimization method, but this optimization method made the minimum Noise Figure is obviously higher than that of noise matching can achieve. Through theoretical analysis, by adding a parallel capacitor, the results of Reference [3] shown that: in low power conditions, the circuit noise can be reduced significantly, but no specific design method is given.On the basis of reference [3], reference [4] gives a concrete design method, however, after the introduction of parallel capacitor, the change of the circuit performance is not clear.

In this paper, based on the input impedance matching,by adding a parallel capacitor achieve low power, and the influence of the shunt capacitance on various parameters of the circuit is analyzed in detail.The simulation was carried out by using Cadence software.

2. 60GHz LNA Circuit

Several main features of the design 60GHz low noise amplifier are as follows: (1) The input impedance of low noise amplifier must be matched into 50Ω, in order to match the 50Ω characteristic impedance of the antenna; (2) The Noise Figure of low noise amplifier should be as small as possible; (3) The gain of the low noise amplifier should be large enough (under the conditions of the system linearity) to suppress the noise of the rear stage; (4) The power consumption of low noise amplifier should be small as well.

In recent years, the design of 60GHz low noise amplifier mainly has two kinds circuit structure, one is the single ended structure, the other is the differential structure.60GHz low noise amplifier needed to

provide a certain gain to suppress the noise of the rear stage, in the mm-wave frequency, with the increase of frequency, the gain Rapid attenuation, so, the gain of a single structure is very small. Reference[6] Simulation of the relationship between the frequency and the maximum available gain(MAG), the results shown that the measured MAG of 90nm NMOSFET is 7.8dB, shown in Fig.1. Even for a cascode configuration, the MAG is only near 10dB due to the low impedance on the inter-stage node. What is more, considering the loss due to the impedance matching network, there is even less gain we can get from a single stage LNA. Therefore, multi-stage topology is needed for LNA to realize a reasonable gain for real application.

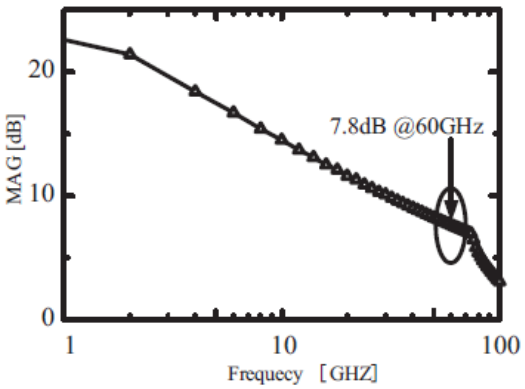
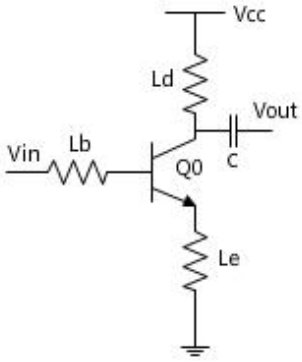


Fig.1 Relationship between the frequency and the maximum available gain

Cascode architecture is widely used for its high gain, good isolation between input and output, making the design more robust and simplifying matching network. However, at mm-wave frequency, due to the low gain of the common-emitter (CE) transistor and high noise of the common-bace (CB) transistor, the noise contribution of the CB transistor increases, which makes cascade topology poor noise performance for 60GHz LNA. Moreover, the gain of cascode architecture, although a few dB higher over CE topology, decreases heavily due to the low impedance on the inter-stage node[10], which makes it even less attractive as the first stage for 60GHz LNA.

Take all condition into consideration, we choose CE as the first stage of the 60GHz LNA,CE transistor with emitter degeneration topology instead of cascode topology as the first stage, not only simplifying matching network, also decreasing the total noise for 60GHz LNA.

CE transistor with emitter degeneration topology is shown in Fig.2, and transistor's small signal model shown in Fig.3.



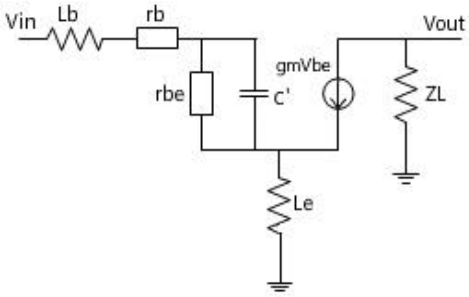


Fig.2 CE with emitter degeneration Fig.3 Small signal model of CE

The input impedance Z_{in} can be calculated from the equation:

$$Z_{in} \approx jw(L_e + L_b) + r_b + \frac{1}{jwC_{be}} + \frac{g_m \cdot L_e}{C_{be}}$$

Set the appropriate value of inductance L_e and L_b to match the input to 50Ω. But in mm-wave frequency, if the value of L_b is too large, the noise performance will be terrible. By adding a capacitor C_p can Improving the total capacitor between the base and the emitter, a capacitor C_p together with the

capacitor C_{be} complete noise matching function and increase the C_p has no effect on power consumption.

The input impedance Z_{in} will be modified as:

$$Z_{in} \approx jw(L_e + L_b) + r_b + \frac{1}{jw(c_{be} + c_p)} + \frac{g_m \cdot L_e}{(c_{be} + c_p)}$$

By adding capacitor C_p, total capacitor of the input stage where get larger,at the frequency of 60GHz, Resonant frequency $w^2=1/LC$. So the value of inductance L_b becomes smaller [5].

Multi-stage topology is used for LNA to realize a reasonable gain. According to the total Noise Figure for multi-stages [6]:

$$NF_{total} = NF_1 + \frac{NF_2 - 1}{G_1} + \ldots + \frac{NF_n - 1}{G_1 \cdot G_2 \cdots G_{(n-1)}}$$

Where NF_i Fand G_i is the Noise Figure and the gain of i stage respectively.

From the equation, we can draw a conliusion that the Noise Figure of first stage determines the noise performance of the whole system. As specified above, CE with emitter degeneration transistors is chosen for the first stages. Cascode stage have been selected to increase reverse isolation and gain. So, the implementation of the first stage is mainly determined by noise considerations. The two cascode stage is needed to increase the overall gain of the LNA. Schematic of the LNA is shown in Fig.4.

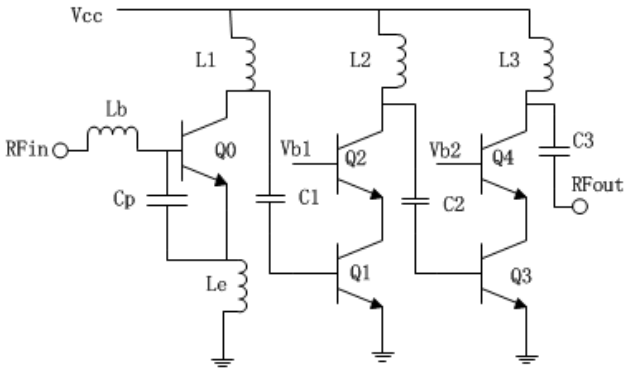


Fig.4 Schematic of the 60GHz LNA

3. Simulations and results

The schematic of the 60GHz LNA has been implemented in 0.18μm SiGe BiCMOS technology. The layout of 60GHz LNA is shown in Fig.5.

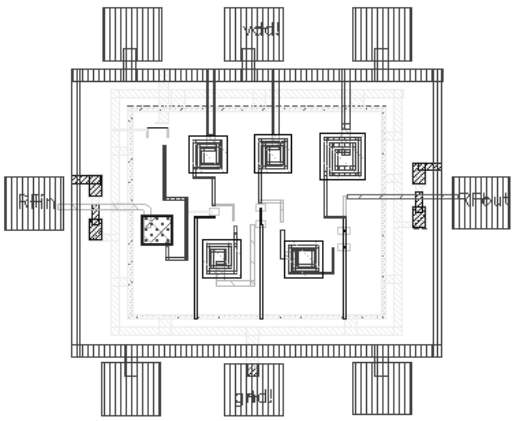
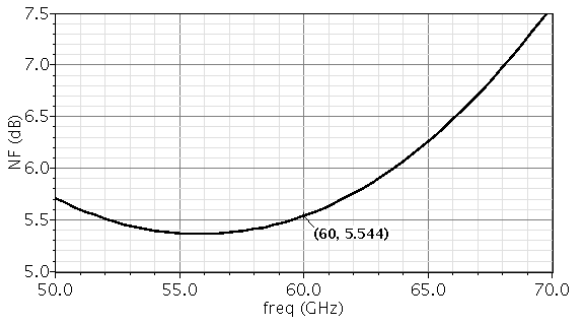


Fig.5 The layout of 60GHz LNA

Make use of Cadence Spectre RF to Simulation. During the simulated process the supply voltage is 3.3V. The simulation Noise Figure, Gain and input/output return loss as shown below.



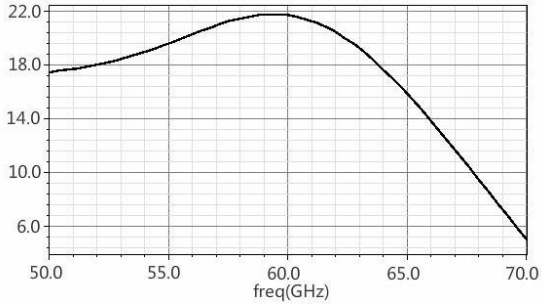


Fig.6 Simulation of Noise Figure Fig.7 Simulation of gain

By adding capacitor C_p, total capacitor of the input stage where get larger, inductance L_b becomes smaller, choosing optimum noise matching and selection bias determined by noise considerations in first stage, all of this make the Noise Figure achieves low target. From the picture in Fig.6, we can see that: in frequency of 60GHz, the simulation Noise Figure is 5.5dB.

The simulation of gain is depicted in Fig.7. The two cascode stage was used to increase gain of the 60GHz LNA. In order to achieves high gain, second stage was bia higher than input stage. The simulation gain is 21.6dB at the center frequency of 60GHz.

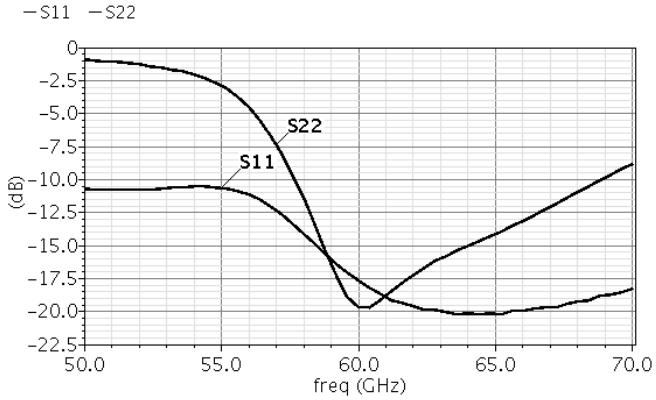


Fig.8 Simulation of S11 and S22

The results of the return losses for input and output show in Fig.8. The simulation S_{11} is -17.5dB at 60GHz and below -10dB from 55GHz-65GHz. Its covers more than 10GHz band. The simulated S_{22} is -20dB at 60GHz. The results shown good input and output matching in this work.

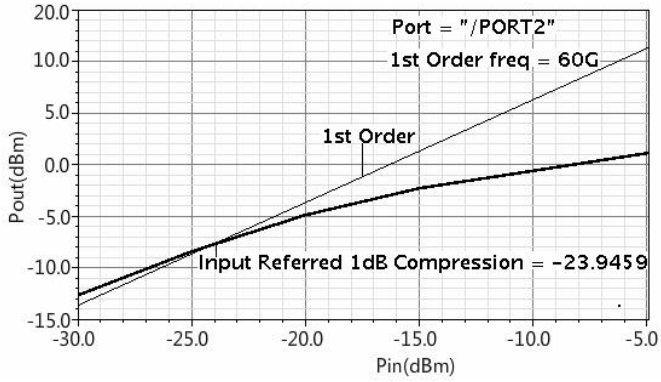


Fig.9 Simulated of P_{-1dB}

Simulated 1dB compression point P-1dB at 60GHz are plotted in Fig.9. The input referred compression point P-1dB is -23.94, the results indicated that the linearity of this work is better

4. Conclusion

A low power three-stage single ended 60GHz LNA was designed in 0.18μm SiGe BiCMOS technology. By adding a shunt capacitance C_p between base and emitter node of CE transistor, the Noise Figure were significantly reduced. In the 60GHz mm-wave frequency, inductors L_b and L_e were used for input impedance matching and without introducing additional noise. From the simulation results,S21 and the Noise Figure are achieved 21.6dB and 5.5dB respectively, input and output return loss S_{11} and S_{22}, lower than -10dB from 55GHz to 65GHz, the power consumption only 12.8mW with the voltage of 3.3V.

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