Design of a Tapped Delay Line Time-To-Digital Converter with 0.18MM CMOS

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Abstract

This paper designed a tapped delay line Time-to-Digital Converter(TDC) based on 0.18μm CMOS, there is total level 128 voltage-controlled delay line.The symmetric delay phase-locked loop is used to increase the stability of delay chain and reduce the system clock's skew and jitter. The simulation results show that : when the voltage is 1.8V, and the reference clock frequency is 250MHz, the least significant bit (LSB) is about 84.6 ps, the effective accuracy (RMS) is about 40.6 ps, the differential nonlinear is -0.7 LSB < DNL < 0.8 LSB, the integral nonlinear is -0.9 LSB < INL < 1.4 LSB.

Keywords

Tapped Delay Line; Time-To-Digital Converter(TDC); D Flip-Flop; Least Significant Bit (LSB).

1. Introduction

Time-to-Digital converter is widely used in measuring two or more time interval signals,its using sections range involved aerospace, high-energy physics, space science, and many other fields. Compared with traditional measuring methods which rely too much on the clock frequency and difficult to achieve higher resolution, time to digital converter has used the interpolation technology, within the time through the division of the measure to achieve higher time resolution.

The design of the TDC implementation methods at now are full custom circuit design based on CMOS and half custom circuit design based on FPGA, although full custom circuit design based on CMOS has long design cycle, high cost disadvantage, but compared to the same technology of half custom circuit design based on FPGA has higher time resolution and better linearity and stability.

Literature [1-3] are tapped delay line circuit, resolution is achieved respectively: 1560 ps and 100 ps and 250 ps; Literature [4, 5] are vernier's delay line circuit, resolution is respectively: 17 ps, 30 ps; Literature [6] is the ring oscillator circuit, the resolution is 156 ps. This paper proposes a tapped delay line time to digital converter based on CMOS, The design of symmetry structure delay phase-locked loop reduced system clock skew and jitter, increases the stability of delay line.

This paper's structure arrangement as follows, the second part expounded the principle diagram of the design of tapped delay line time to digital converter and the measuring principle briefly, the third part introduces the voltage-controlled delay unit, edge-triggered D flip-flop, phase discriminator and the design of the charge pump, the fourth part introduces the circuit's layout design and simulation analysis, At last, summarized.

2. Tapped delay line Time-to-Digital Converter

At present, in the using of interpolation technology in many fields, the gate delay as the basic unit of time delay technology can improve the resolution of time to digital converter significantly, the tapped delay line's way of interpolation is gate delay,as the basic unit, the time resolution is determined by the gate delay time, the smaller the gate delay time get the higher the time resolution, and the more delay unit linked in the delay line the measuring range will be greater, this paper's design of tapped delay line time to digital converter's main modules are voltage-controlled delay chain, edge-triggered D-flip-flop, phase discriminator and charge pump, the overall structure diagram is shown in figure 1.

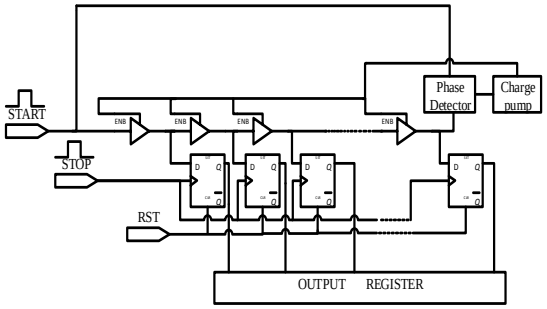

Fig. 1 Tapped delay line time-to-digital converter

The start signal linked with delay unit and edge-triggered D flip-flop's input, the start signal will generate the corresponding time delay when get through each delay unit, the stop signal connect with edge-triggered D-flip-flop's clock port as a trigger signal, when the stop signal's rising edge arrive, D-flip-flop sampling the start signal and quantifying the time by the number of time delay unit it got through. The measurement sequence diagram is shown in figure 2.

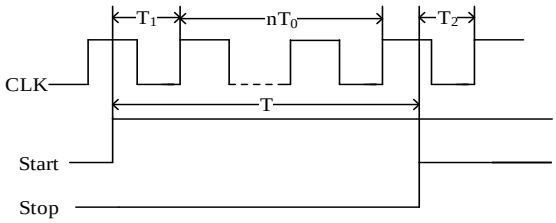

Fig.2. TDC measure sequence diagram

Time formula shown as (1):

$$T = T_1 + nT_0 + (T_0 - T_2) \tag{1}$$

Where n represents complete cycle number between the start signal and the stop signal , measured by the counter. T_0 represents standard clock cycles, nT0 means crude measuring time. Precision measuring time T_1 and T_2 represent the time interval between start and stop signal's rising edge with the next clock signal's rising edge respectively. which can be calculated as the number of delay unit which get through tapped delay line's start signal multiply the delay unit's resolution, the CMOS tapped delay line's fine time measurement formula shown as (2):

$$T_f = nT_{LSB} \tag{2}$$

The Tf (T1,T2 are all expressed in Tf here) represents time interval, n represents the number of delay unit which start signal get through TLSB means delay unit's time resolution, quantitative error produces in the process of measuring system, due to the limited resolution system, quantitative error can't be eliminated exactly, only can be reduced the effects through correction formula significantly. because of

So there is the correction formula(3):

$$T_f = nT_{LSB} + \frac{1}{2}T_{LSB} \tag{3}$$

Quantization error's range of variation after correction formula is (), then measure repeatedly and take the average we will get the time interval data more accurate.

3. The design of TDC delay line's main module

3.1 Voltage-controlled delay unit's design

In order to make the delay time change smoothly when delay unit's control voltage change, this paper use NMOS voltage-controlled delay unit to design the voltage-controlled delay line, the structure is shown in figure 3.

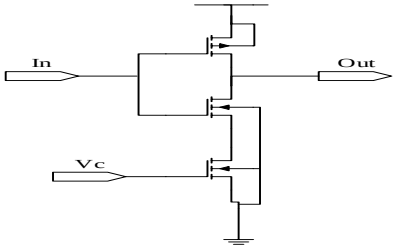

Fig.3 Voltage-controlled delay unit

The delay time's change with the control voltage is shown in figure 4.

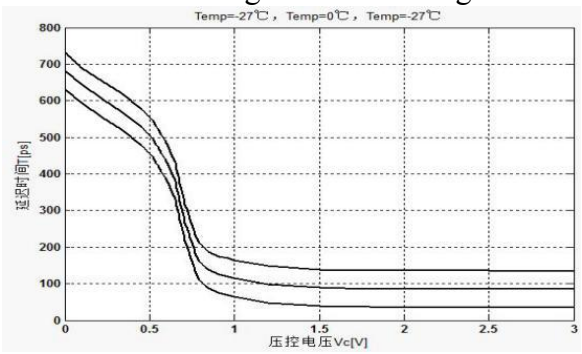

Fig.4 The control voltage - delay time

3.2 Edge-triggered D-flip-flop's design

In order to improve the reliability and anti-interference ability of D flip-flop, this paper chooses two level trigger D flip-flop to compose of one edge-triggered D flip-flop, which structure is shown in figure 5.

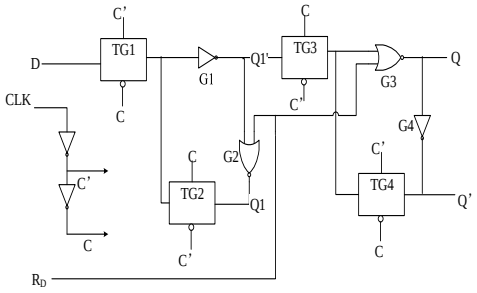

Fig.5 Edge-triggered D flip-flop

The D flip-flop's minor state only depends on the input signal's state when arrival of the clock signal's rising edge, its anti-interference ability being enhanced effectively.

3.3 Phase discriminator and charge pump's design

Phase discriminator and charge pump circuit are designed to reduce the clock skew and jitter. Phase discriminator use symmetrical structure to guarantee a small phase imbalance, even working in a high frequency environment. which structure is shown in figure 6.

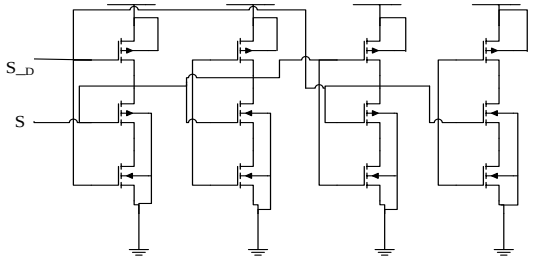

Fig.6 Phase discriminator

Phase discriminator produce the UP or DOWN pulse signal by comparing the phase difference between the START signal and the output signal which pass the final level of voltage-controlled

delay unit. If the START signal ahead of the output signal, Phase discriminator will generate the pulse signal of UP, conversely, DOWN pulse signal will be generated. The pulse signal will be sent to the Charge pump so that it can change the controlled voltage and adjust the delay time of the voltage-controlled delay unit in the same time. In addition, there is a small bunch of pulse signal keeping the latch state to reduce the dead zone time of Phase discriminator [7]. Charge pump's circuit diagram is shown in figure 7.

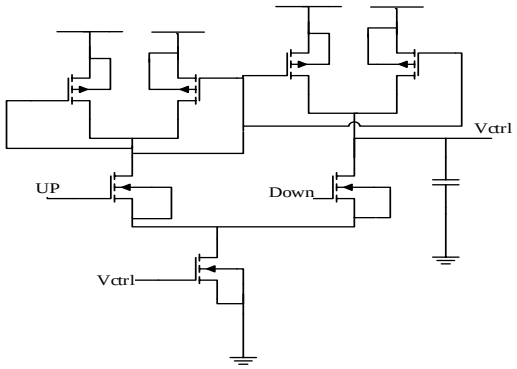

Fig.7 Charge pump

Charge pump is composed of double NMOS source coupling and current mirror circuit which composed of symmetrical load unit. When comes the UP or DOWN signal, the capacitor will guarantee the stability of system's delay time by means of charging or discharging [8].

4. The circuit's layout design and simulation analysis

This paper use cadence virtuoso software platform to complete 128 level tapped delay line TDC circuit's layout drawing and simulation test, the layout is shown in figure 8.

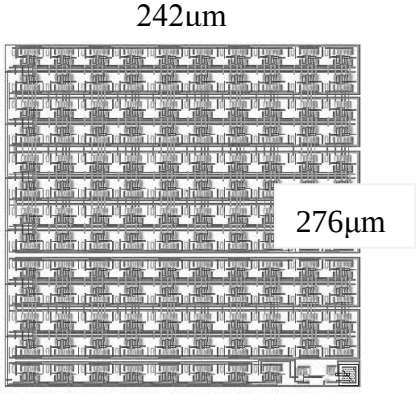

Fig.8 TDC circuit's layout

At 0℃ simulation environment, 1.8 V control voltage , 250 MHZ reference clock frequency, the is 84.6 ps, statistical analysis result shows that the RMS is about 40.6 ps effectively. Differential nonlinear expressed by formula (4).

$$DNL_i = \frac{d_{i+1} - d_i - T_{LSB}}{T_{LSB}}, i = 0,1...N-1 \quad (4)$$

And the integral nonlinear expressed by formula (5).

$$INL_i = \frac{d_i - i * T_{LSB}}{T_{LSB}}, i = 0,1...N-1 \quad (5)$$

Formula (4), (5) represent the first tap to the n tap's delay time, represents the average delay time of each tap [9]. Based on the circuit's simulation delay data and the formula (4), (5) we can get DNL, INL diagram as shown in figure 9, 10.

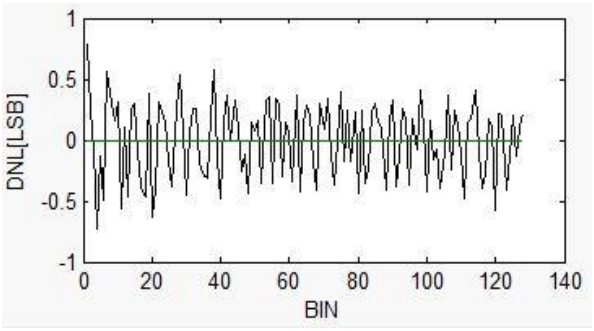

Fig.9 DNL

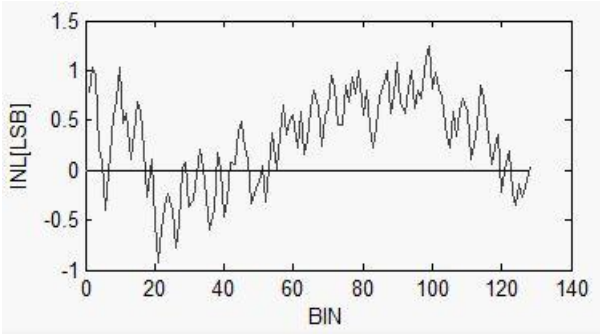

Fig.10 INL

From figure 9, 10 we know the delay unit's DNL scope is (0.7, 0.7) LSB, and have a good consistency. INL scope is (0.9, 0.9) LSB, Table 1 is the main performance parameters' comparing of this paper to others'.

Table 1. Comparison with Other TDCs

Ref	[3]	[4]	This paper
Architecture	Counter and delay lines	Counter and Vernier	Counter and delay lines
TEC (μm)	0.5	0.09	0.18
LSB (ps)	250	17	84.6
RMS (ps)	72	N.A	40.6
DNL (LSB)	(-0.08,0.08)	(-0.6,0.6)	(-0.7,0.8)
INL (LSB)	(-0.1,0.1)	(-0.8,0.8)	(-0.9,1.4)

5. The total

This paper design a 0.18 μm CMOS tapped delay line structure to make the TDC has high time resolution and RMS, The using of delay phase-locked loop has greatly reduced the system clock's skew and jitter, enhances the system's stability.

Further analysis, the first delay unit's large delay time lead to a major DNL, and successively, the delay unit's delay time beyond (or below) average delay time lead to the INL curve's fluctuates. Continuously accumulate also result in the INL more than 1 LSB, optimal method should be found in the follow-up work.

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