The Real‑Time Spectrum Analysis Algorithm for the Weak Signal under Strong Noise Background and its Implementation on FPGA Platforms

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Abstract

The traditional spectrum analyzer does not have the function of real-time spectrum detection and inadequate capacity of analyzing the weak signal under strong noise background, so a real-time spectrum analytical approach is presented and implemented on FPGA hardware platform in this paper. A double channel ADC time interleaved parallel sampling, signal power extraction, frequency template triggering, poly-phase filter, spectrum zooming of Chirp Z Transform and spectrum analysis are adopted in this method to achieve the real-time spectrum analysis of signal. The configuration clock frequency of FPGA can be calculated according to the system delay analysis and the input arguments. The simulation result proves that this method can not only overcome the problem of traditional methods, based on power trigger and level triggered sampling, which have weak analysis ability of weak signal under strong noise background, and can not achieve specific frequency interval analysis, but also overcome the defects of mutual restriction between time-frequency resolution. For weak signal, it has a frequency measurement error less than 0.6% and power error less than 4.5%, the maximum system time delay is less than 37μs. Except for 22.558μs initial time delay, this design has the property of real-time processing of continuous data.

Keywords

Real-Time Spectrum Analysis, Poly-phase Filter, Chirp Z Transform,Weak Signal, System Delay.

1.　introduction

In the field of industrial monitoring, the method about judging the running condition of the rotating electromechanical equipment and the real-time fault detection through the analysis of the power spectral characteristics of vibration signals and noise signals related to shaft rotation frequency in rotating equipment is a very effective[1]. Therefore, frequency spectrum analysis is an important task in most disciplines, and the main objective is power spectrum measurement. Traditional methods of spectrum analysis are usually adopting power triggering or level triggered triggering. Besides, FFT and its improved algorithm or spectral Zoom Spectrum analysis method are adopted. FFT algorithm obtains a rough panoramic spectrum of the whole analysis frequency band, and using the frequency thinning algorithm can obtain the local detailed features of the spectrum. Considering frequency spectrum characteristic of the weak signal under strong noise background, hardware complexity and real-time. In this paper, FFT algorithm is used to obtain the signal spectrum profile to implement frequency template triggering, and then use the poly-phase filter to obtain analysis frequency band signal reconstruction, implement the spectrum refinement which is independent of time resolution through windowed CZT, and solve the side-lobe spectrum analysis error and noise error by using the cumulative mean and the spectrum analysis, and finally implement it on FPGA Platforms.
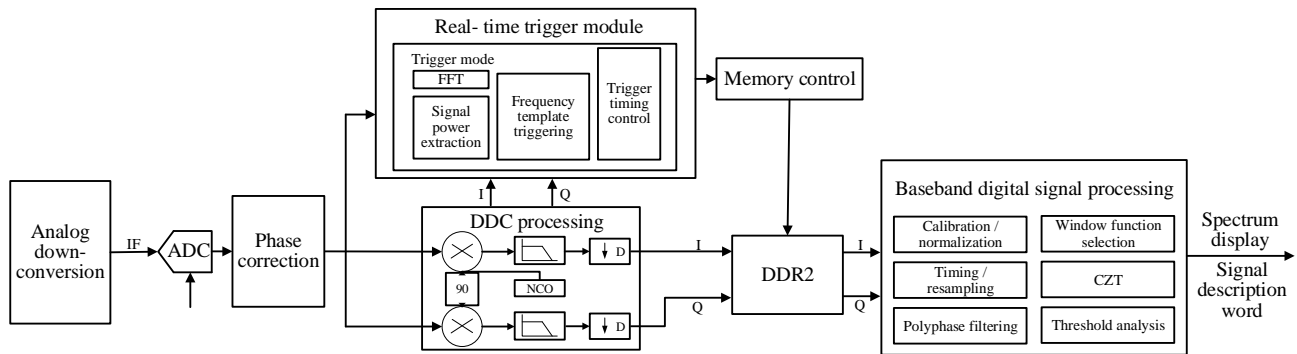
2. System overall design

Fig.1 Global View of Spectrum Analyzer

A global view of the design is shown in Fig.1. After analog down-conversion and ADC sampling, the RF signal is sent to FPGA to implement channel mismatch correction, DDC, real-time trigger control, memory control and baseband digital signal processing. In the real-time trigger module, FPGA firstly uses FFT to make the time-frequency conversion of the input signal, and then uses the data preprocessing module to extract the signal power, and then triggers the decision and timing. According to the trigger timing control of the real-time trigger module, the memory control module sends the captured valid data from the memory to the baseband digital signal processing module for real-time spectrum analysis. Baseband digital signal processing module uses poly-phase filter banks to realize user selection of frequency sub-band filtering and the simulation of long observation window to improve the frequency resolution. The appropriate window is used to ensure the frequency resolution and dynamic range requirements, by using CZT obtains the spectrum refinement, which is independent of time resolution, and the local spectrum zoom. Threshold analysis module can analyze the output spectrum of CZT and display the number of signals contained in the spectrum, center frequency of each signal and the signal description word(SDW) in the table form.

3. Analysis and implementation of key modules

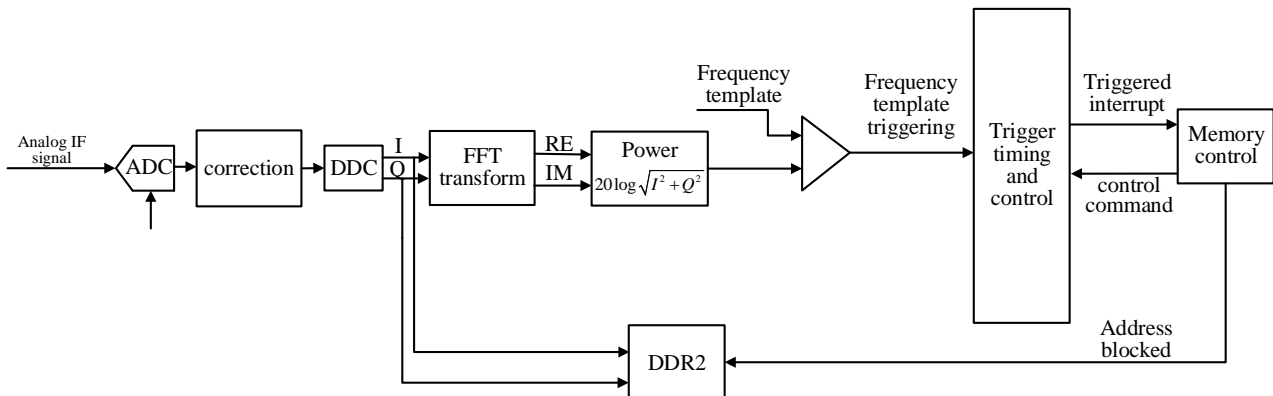### 3.1 Frequency trigger template principle and FPGA implementation

Fig. 2 structure chart of spectrum trigger template

The unit of frequency trigger module is data frame, the data through the digital down-conversion is divided into two parts. One part of data after FFT transform is used to extract the power of the square of the output complex spectrum modulo for comparison with trigger templates, if the power of a point signal, which is through the FFT transform, in power spectrum is larger than the corresponding power threshold of the frequency template, it will produce trigger. Another way the data is seamless captured directly, stored in DDR2 and wait for the trigger to generate. When the trigger occurs, by using the trigger control and timing module, manage the trigger memory addresses, and control instructions about the data in memory to write, freeze and read, and the sent the data to baseband

digital signal processing module to make a real-time spectrum analysis. The FPGA implementation status transition is shown in fig. 3.
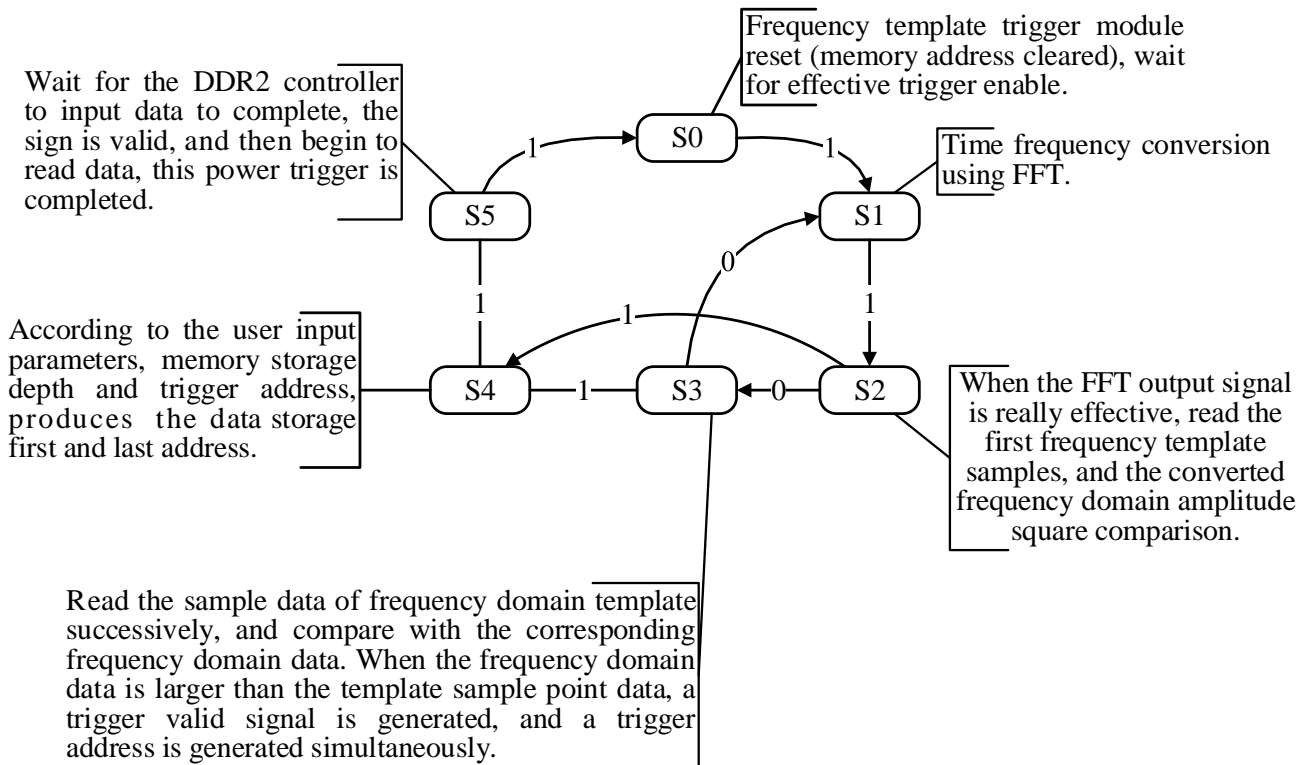
Wait for the DDR2 controller to input data to complete, the sign is valid, and then begin to read data, this power trigger is completed.

Frequency template trigger module reset (memory address cleared), wait for effective trigger enable.

Time frequency conversion using FFT.

According to the user input parameters, memory storage depth and trigger address, produces the data storage first and last address.

When the FFT output signal is really effective, read the first frequency template samples, and the converted frequency domain amplitude square comparison.

Read the sample data of frequency domain template successively, and compare with the corresponding frequency domain data. When the frequency domain data is larger than the template sample point data, a trigger valid signal is generated, and a trigger address is generated simultaneously.

Figure 3 spectrum triggered template FPGA to achieve the state transition diagram

3.2 CZT algorithm principle and FPGA implementation

The combination and corrected sampling signal $x(n)(n = 0, \cdots, N-1)$ are realized by FPGA. According to the literature [2], the Z transform can be expressed as:

$$X\left(z_k\right) = W^{k^2/2} \sum_{n=0}^{N-1} f\left(n\right) h(k-n) \tag{1}$$

Where $f(n) = x(n) A^{-n} W^{n^2/2}$, $h(n) = W^{-n^2/2}$, $A = A_0 e^{i\theta_0}$, $W = W_0 e^{-i\varphi_0}$. A_0 is the amplitude of the starting point for the z plane, θ_0 is the phase of the starting point (corresponding to the frequency of the starting point), W_0 is the reciprocal of the amplitude gradient and φ_0 is the phase increment (corresponding to the frequency resolution). $A_0 = W_0 = 1$, the CZT transform path is a section of circular arc on the unit circle, M=N (M is the number of spectral lines), and simplifies the computational complexity of CZT. By using θ_0 to adjust the starting frequency, and by using φ_0 to determine the refinement ratio in the range of frequency selection.

The core of formula (1) is convolution calculation between $f(n)$ and $h(n)$. By the convolution theorem of Fourier transform, it can be concluded that cyclic convolution can be computed rapidly by FFT [3]. According to the CZT principle, the signal is related to input frequency, termination frequency, thinning factor and output line number. Therefore, the signal generation can be realized by two DDS modules and a data buffer RAM. In order to improve the system operation speed, the two DDS modules and two FFT are implemented in parallel architecture. In order to save resources and improve chip utilization, complex multiplier is multiplexed and multiplex FFT1 to FFT3. At this point, the FPGA implements the CZT module data flow, as shown in fig. 4.
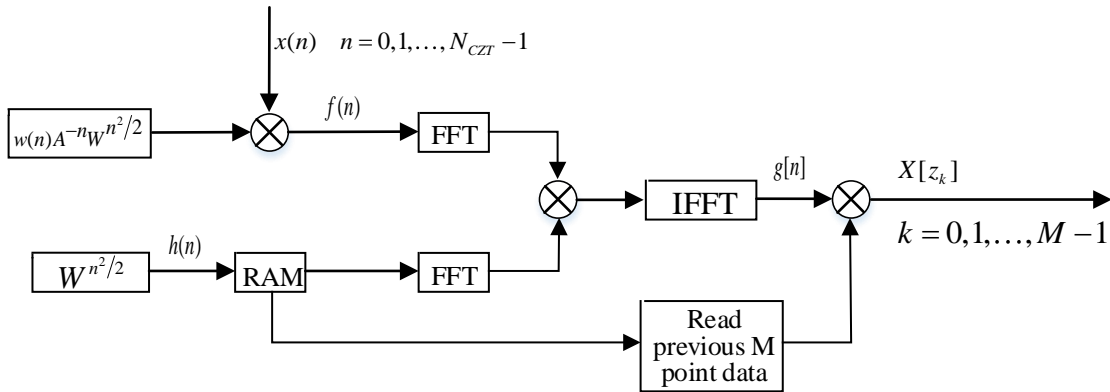
Fig.4 Data flow diagram of CZT algorithm hardware implementation data flow diagram

3.3 Window selection principle and FPGA implementation

The window choice is the most critical aspect of ensuring the successful application of the algorithm. The normalized frequency resolution of the system can be expressed as $\Delta f_b = \Delta f / \Delta f_1 = \Delta f \cdot M / (f_{max} - f_{min}) = \Delta f \cdot ND / f_s$, where D is frequency refinement multiples, The window must satisfy the following conditions:

1) Window SLL (sidelobe level) must satisfy: SLL > IDR. Otherwise, the algorithm will not be able to meet the IDR requirements.

2) The 6dB bandwidth of window needs to be satisfied: $BW_{-6dB} < \Delta f_b$. To accomplish this situation when the frequency resolution is Δf, and correctly distinguish two signals of the same power, the typical standards $BW_{-6dB} < \Delta f_b$ are adopted[4].

3) Window amplitude drops, IDR dB bandwidth needs to be satisfied: $BW_{IDR} < 2\Delta f_b$. To ensure the detection of a signal separated Δf from another signal IDR dB which has more power, the corresponding window width of the IDR must be narrower than $2\Delta f_b$.

In order to accomplish accurately detection of N_s signals, the worst side-lobe condition (i.e., the input signal is the combination $N_s - 1$ same power signals with another signal whose power is IDR dB below) should be considered, and the window should satisfy the following conditions:

$$SLL > IDR + 20\log_{10}(N_s - 1) + SL \tag{2}$$

where $N_S > 1$. The SL is window scalloping loss,i.e, the power loss when the signal frequency is located between two CZT frequency points[5].

According to the requirements of IDR, the normalized frequency resolution can be expressed as:

$$\Delta f_b = \frac{BW_{-IDR}}{2} = \frac{BW_{null}}{2} \tag{3}$$

Where BW_{null} is the window main lobe width in bins.

3.4 Principle of spectral analysis algorithm and FPGA implementation

In order to reduce the measurement error and obtain more accurate measurement results, three threshold parameters are designed in this paper. In this section, the threshold parameter setting theory is discussed in detail, and the specific parameters are shown in figure 5.
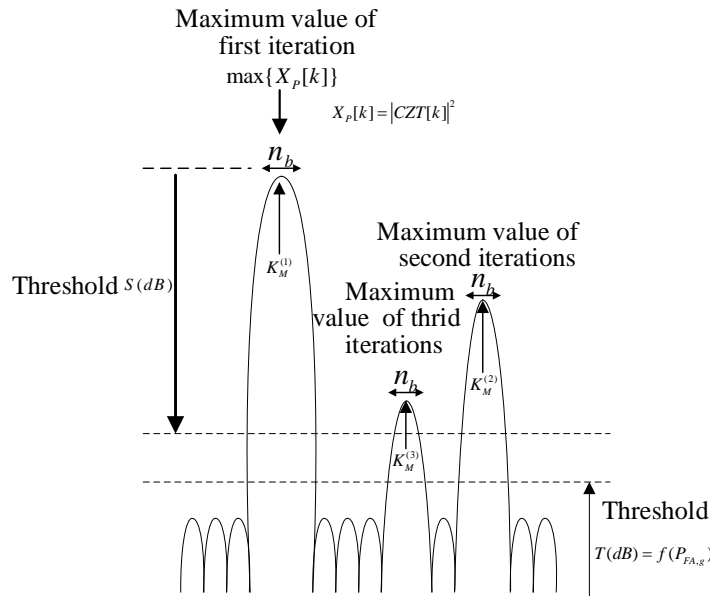
Fig.5 The Schematic diagram of Threshold parameter

1) window main width valve n_b : To simplify the hardware implementation of the algorithm, the main lobe of the signal after adding windows is assumed to be composed of odd point CZT resolution points, $n_b = 2\lceil BW_{null}/2\rceil + 1$. To avoid the situation that n_b is the even, reduce the error detection probability and eliminate the both side of the signal maximum $n_b/2$ or $(n_b - 1)/2$.

2) Noise threshold T dB: In order to avoid the measurement error caused by noise, the noise threshold T (dB) is introduced here. Defined according to document [5]:

$$P_{FA} = e^{-T/\sigma_T^2} \tag{4}$$

where P_{FA} is the fixed value related to noise power σ_T^2 and the error detection probability caused by noise. If σ_T^2 is known, suppose $X_P[k]$ is the power value which is located in k bins, M is the only noise power point, γ is related to the global error detection probability $P_{FA,g}$, then the threshold T can be expressed as:

$$T = \gamma \frac{1}{M}\sum_{k=1}^{M} X_P[k] \tag{5}$$

When $M \gg 1$, plug the formula (5) into (4):

$$P_{FA}\big|_{M \gg 1} \approx e^{-\gamma} \tag{6}$$

At this point, P_{FA} detector performance tends to the ideal detector (4).

If the number of spectral lines is M_{CZT} and obeys independent and identical distributed, then

$$P_{FAg} = 1 - (1 - P_{FA})^{M_{CZT}} \rightarrow P_{FA,g}\big|_{P_{FA} \ll 1} \approx M_{CZT} P_{FA} \tag{7}$$

According to formula (6)、(7), it can be known :

$$\gamma \approx -\ln(P_{FA,g}/M_{CZT}) \tag{8}$$

Dynamic threshold S (dB): In order to ensure the requirements of IDR, avoid the detection error caused by the secondary lobe of the window, so set the dynamic threshold $S = IDR + SL$, in which SL is the scalloping loss of the window.

By cumulative averaging the output data of the CZT module, the transient error is reduced. And the results are sent to make a spectrum analysis to obtain SDW. The specific implementation steps are shown in figure 6.
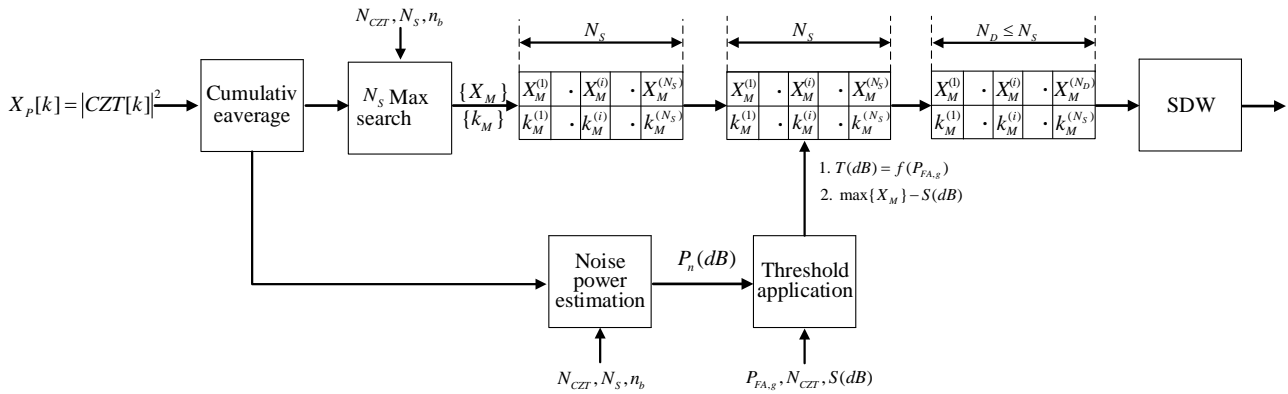
Fig.6 The structure diagram of Spectrum Analysis

Create two memory whose length are N_s, storing power values and corresponding data locations, respectively. Spectral analysis can be achieved by the following steps:

Output the CZT result of M point, according to the parameters n_b to find the N_s maximum points, and its power and location corresponding to storage. In FPGA, by reading the cumulative average data in cache RAM, and searching the maximum point by the comparator in turn, the power value and the corresponding location are stored respectively. When the maximum value $k_M^{(i)}$ is found in the i iteration, $(n_b-1)/2$ point data of $k_M^{(i)}$ both the left and right are discarded at the time of reading, and the read result is written to the next level cache RAM. Similarly the same signal power spectrum data can be obtained.

2) Noise estimation: the noise power is not considered as the N_s average of the output power associated with the signals above :

$$P_n = \frac{1}{M_s}\sum_k X_P[k]b[k] \tag{9}$$

where (9), $M_s = M - n_b N_s$. $b[k]$ is the blank window:

$$b[k] = \begin{cases} 0 & k = k_M^{(i)} - (n_b-1)/2,\ldots,k_M^{(i)} + (n_b-1)/2, i=1,\ldots,N_s \\ 1 & 其他 \end{cases} \tag{10}$$

where (10), $k_M^{(i)}$ is the i storage value in the position memory.

3) Threshold application: according to the principle and noise estimation results above, noise threshold $T = P_n(\text{dB}) + 10\log_{10}(\gamma)$ and dynamic threshold $10\log_{10}(X_M^1) - S(\text{dB})$ can be calculated and applied. The signal parameters in the memory need to make the logarithm operation, read and compared with the noise threshold and the dynamic threshold sequentially. When the signal power is less than the threshold, it is discarded or otherwise reserved.
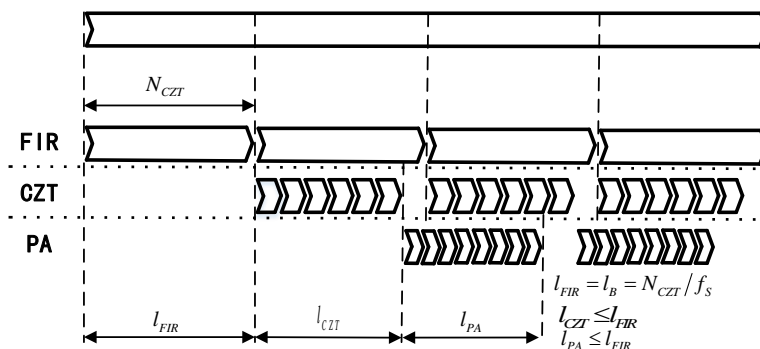
3.5 System delay

Fig.7 The Schematic diagram of Spectrum Analyzer Time-Delay

Mathematical operations of baseband digital signal processing module mainly focused on three sub modules: multiphase filtering, CZT and threshold analysis. To achieve the pipeline processing of baseband digital signal, the design of the three modules of the data flow diagram as shown in fig.7. Two latency are defined here: latency between blocks l_B (the time interval in when a new block can be introduced in the system) and the total delay l_T (the time interval to obtain the block result SDW when the first sample is introduced). According to fig.7, $l_T = l_{FIR} + l_{CZT} + l_{PA}$, therefore, $l_B < l_T$. Since the modules are pipelined, the next block of data can enter the system before the previous block of data is processed. The time delay of the poly-phase filtering module is reconstructed from the resampling data filtering into the data block whose frame length is N_{CZT}, and the processing time is N_{CZT} clock cycle and N_{CZT} window is added to the clock cycle, so l_B can be expressed as:

$$l_B = \frac{NT + N_{CZT}}{f_s}$$ (11)

The poly-phase filter module processes the data continuously at the sampling rate f_s and stores the results in the First input first output (FIFO) memory, so the delay of the module is equal to the block delay, $l_{FIR} = l_B$. When the first data block passes through the poly-phase filtering module, the CZT module will start to process the data, so the CZT module must process the data block before the next data block completes the poly-phase filtering, it means $l_{CZT} \leq l_{FIR}$. The delay of CZT module consists of 10 cycles address arithmetic delay, 3 cycles complex multiplier, N_{CZT} cycles FFT and N_{CZT} cycles IFFT delay, l_{CZT} can be expressed as:

$$l_{CZT} = \frac{2 \cdot N_{CZT} + 13}{f_{CZT}}$$ (12)

Before the CZT module loads a new set of data, the spectral analysis module should complete the previous set of data processing, which means $l_{PA} \leq l_{FIR}$. Spectrum analysis first need to load the output data of CZT module into the spectrum analysis module, and then make N_s maximum search of N_{CZT} CZT output results, a noise estimation and 280 clock cycles of the other treatments (spectrum adjustment and SDW generation). However, because the cumulative average and maximum search is based on 1 cumulative RAM and 5 cache RAM implementations, the spectral analysis delay l_{PA} can be expressed as:

$$l_{PA} = \frac{N_{CZT} + 280}{f_{PA}}$$ (13)

Through the above module delay analysis, $l_T \leq 3 \cdot l_{FIR}$ can be seen.

4. System verification

In this section, we will verify the performance of the spectrum analyzer in the weak signal under strong noise background. The hardware platform uses Altera, Cyclone, IVE: EP4CE115F29I7 and FPGA.

In order to verify the detection performance of weak signal under strong noise background, the test signal is produce by MATLAB:

$$x_1(i) = \begin{cases} \sin(2\pi f_1 i / f_s) + 0.5\text{randn(size(i))} & i \in [1, 2048] \\ \sin(2\pi f_1 i / f_s) + 0.02\sin(2\pi f_2 i / f_s) \\ + 0.5\text{randn(size(i))} & i \in [2049, 5120] \end{cases}$$

Where: $f_1 = 44\text{MHz}$, $f_2 = 65\text{MHz}$, $f_s = 200\text{MHz}$, and randn is zero mean random noise signal. Since the weak signal frequency is 65MHz, MATLAB is used to generate a frequency spectrum template with a trigger frequency of 56.65MHz~68.75MHz and a normalized amplitude of 0.00032.

Based on the analysis of bandwidth and filter sub-band bandwidth, the filter sub-bands 7 and 10 are selected in this example. And the buffer delay period is set to 0 because the test signal is a stationary signal. In order to satisfy the performance of real-time spectrum analysis, the clock of CZT module

and threshold analysis module should be set properly. According to document [6], the maximum frequency of the FFT module is $f_{FFT} = 400\text{MHz}$,therefore, $f_{CZT\max} = 400\text{MHz}$. By formula (11), $l_{FIR} = l_B = 5.12\mu s$ can be obtained. By formula (12) and continuous data stream processing module of CZT timing constraints, $f_{PA\min} = 154.69\text{MHz}$ is available. By formula (13) and the timing constraints of continuous data stream processing threshold analysis module, $f_{PA\min} = 154.69\text{MHz}$ is obtained. According to $f_{CZT\max} = 400\text{MHz}$, $f_{PA\max} = 310\text{MHz}$ can be concluded. Therefore, to meet the requirements of the clock frequency as listed in table 1.Considering the system clock frequency is 300MHz, the system power consumption is reduced, and the real-time processing of the signal flow is guaranteed. In this case, $f_{CZT} = 250\text{MHz}$, $f_{PA} = 200\text{MHz}$, the CZT and threshold analysis module are configured, and the system delay $l_T = 13.23\mu s$ is achieved.

As the user input $IDR = 30\text{dB}$, $N_s = 2$, according to the formula (2) can be seen, $SLL \geq 32$. The window is selected Hamming window (according to document [4], Hamming window, SSL=-43dB, SL=1.78dB and main valve count =4) to meet the requirements of IDR, and $n_b = 5$, $S = 32\text{dB}$. According to the starting and stop frequency, and the sampling rate of the system, $D = 8$ can be seen. The normalized resolution formula, frequency resolution and formula (3), $N_{CZT} = M = 512$ are obtained. According to the relation between the initial frequency, the initial phase and $N_{CZT} = 512$, $\theta_0 = 2\pi \times f_{\min} / f_s = 2\pi \cdot 86/512$, $f_{PA\max} = 250\text{MHz}$ is obtained. Use $f_{CZT} = 400\text{MHz}$, $f_{PA} = 250\text{MHz}$ to configure the CZT and PA modules, the system delays $l_T = 38.27\mu s$.

Table 1. baseband digital signal processing module clock configuration (weak signal performance test)

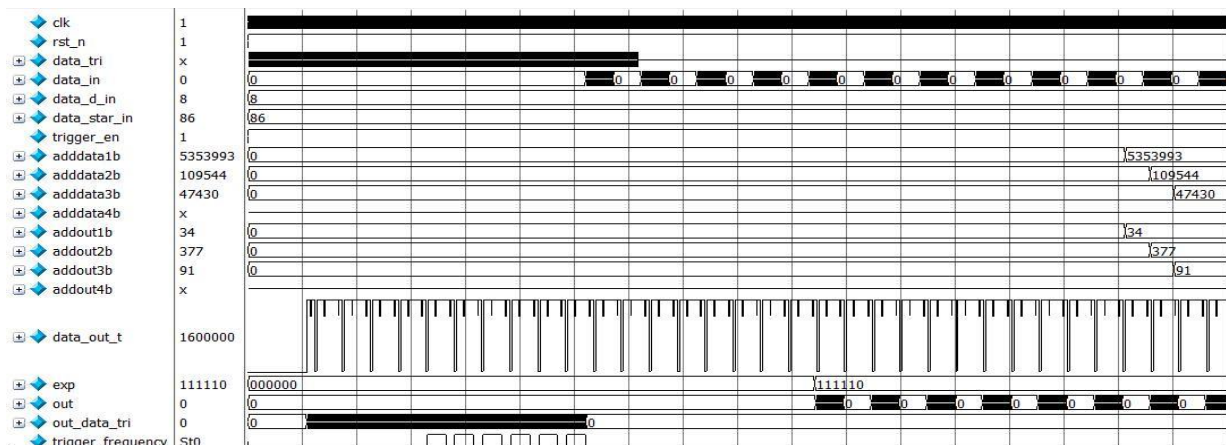| CZT and threshold analysis module total delay		f_{CZT}(MHz)		
		250	300	400
	200	8.108	7.417	6.553
f_{PA}(MHz)	250	7.316	6.625	5.761
	300	6.788	6.097	5.233

Fig.8 The timing simulation waveform of weak signal

The frequency values and power values of detection signals can be obtained from Fig.8. The input and detection signal frequencies and normalized power values are shown in table 2.

Tab.2 Comparison of weak signal measurement results

	44	65
Input signal frequency f_{in} (MHz)	44	65
Measuring signal frequency f_{test} (MHz)	44.07	65.01
Absolute error(MHz)	0.07	0.01
Normalized amplitude of input signal A_{in}	1	0.02
Normalized amplitude of measured signal A_{test}	1	0.0205
Relative error (%)	0	2.5

5. Conclusion

Based on the advantages of frequency template triggering method and CZT algorithm, the real-time measurement of weak signal under strong noise background power spectrum, a real-time spectrum based on frequency mask trigger and poly-phase filter bank, CZT transform and spectrum analysis of a combination of easy hardware implementation method is presented in this paper, and make a hardware implementation of this method by using FPGA platform. This method uses a frequency template to achieve a specific frequency range triggering, poly-phase filtering reconstruct the user focus spectrum, the CZT spectrum zooming algorithm to solve the limited window length on frequency resolution, spectral analysis algorithm provides accurate results of the spectrum analysis. The analysis result shows that the system can accurately detect the weak signal under strong background noise and spectrum analysis of the simulation results and error detection, the frequency error is less than 0.16% (70KHz), power error is less than 2.5% and the minimum delay system is less than 37 μs. Simulation analysis shows that the design has good detection accuracy, time-frequency accuracy and real-time performance for weak signal frequency spectrum analysis.

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