Design and Implementation of DDFS Based on Quasi-linear Interpolation Algorithm

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Abstract

In this paper, a quasi-linear interpolation algorithm which can be applied on DDFS is proposed. And the hardware design is achieved on FPGA. The core block of DDFS is the phase-to-sine mapper (PSM). The advantages and disadvantages of the different PSM algorithms is discussed. The piece-wise fitting algorithm for sine wave curve utilizing linear functions and parabolic functions, which improving algorithm precision and decreasing the algorithm complexity effetely. The algorithm is useful to improve the speed of the hardware. The fitting result is analyzed with MATLAB. According to the circuit performance requirements, the polynomial coefficients are got. The Altera's Cyclone II device is used for implementation. The experimental results show that: the frequency resolution of DDFS is as high as 7.45e-7Hz, and the spectral purity is high, its SFDR value is -94dBc.

Keywords

Direct Digital Frequency Synthesizer(DDFS); Quasi-linear interpolation algorithm; FPGA.

1. Introduction

Digital Direct Frequency Synthesis (DDFS) technology was proposed by J. Tirency [1] in 1971 and is a new digital frequency synthesis method [2] based on phase concept. Direct simulation frequency synthesis and phase-lock link frequency synthesis (PLL [3]), are also the key technologies to realize all-digital equipment [2]. Compared with traditional frequency synthesis techniques, DDFS has the advantages of short switching frequency, high frequency resolution, and continuous phase variation [4], making DDFS widely used in radar, software defined radio (SDR), communications, biology Medical testing equipment and other fields [4].

Since DDFS technology was put forward, domestic and foreign scholars have been perfecting DDFS theory continuously, and introduced various algorithms, which are mainly divided into four types: angle decomposition algorithm [6], sine amplitude compression algorithm [6][7], angle rotation algorithm [8], polynomial approximation algorithm [1].

Angle decomposition algorithm [6] is based on trigonometric approximation formula trigonometric function expansion, and then different sections of the ROM corresponding to different look-up table [1]. This method is intuitive but is limited by the trigonometric identities and approximation formulas and is difficult to angle decompose. Sine Amplitude Compression Algorithm [1] [6] [7] reduces ROM memory by storing an error function in the ROM look-up table. The method is simple in structure but requires the introduction of a ROM look-up table for storing error correction functions. The above two methods are all based on the DDFS of the ROM look-up table. However, as the word length of the DDFS phase accumulator increases, the size of the ROM look-up table can be very large. The circuit design has the disadvantages of high power consumption, slow speed and difficulty in implementation. Therefore, in recent years, the design of DDFS has focused on reducing the ROM look-up table size and even replacing the ROM look-up table. So there are angle rotation algorithm and polynomial approximation algorithm.

Angle rotation algorithm [8] is mainly based on CORDIC algorithm [1], this method can fundamentally reduce the ROM look-up table capacity or even replace the ROM look-up table, but the delay, the system operating frequency is low, the output waveform Small bandwidth [9].

In order to overcome the shortcomings of the above three methods, the polynomial approximation algorithm is proposed [4], that is, from the phase point of view, through the piece-wise polynomial calculation, the synthesis of the required frequency sine wave. The method achieves high purity of DDFS spectrum, low power consumption and high sampling precision. It can be divided into three categories: first-order polynomial approximation algorithm [4] [5], second-order polynomial approximation algorithm [2] and higher-order polynomial approximation algorithm.

This paper intends to use a new class of linear polynomial algorithm to reduce the complexity of the algorithm, while ensuring high accuracy. And the algorithm on the FPGA hardware design. The first section of this article analyzes the working principle of DDFS and the limitations of traditional algorithms. The second section analyzes the linear interpolation algorithm. The third section discusses the FPGA design of the algorithm. Concluded the conclusion.

2. DDFS structure and working principle

A complete DDFS system consists of phase-accumulator (PAC), phase-to-sine mapper (PSM), digital to analog converter (DAC) and low The pass filter (LPF) four parts constitute [1] [2] [4] [5], the output is a sine wave. The block diagram shown in Fig. 1, the input and output signals are defined in Table 1 below.

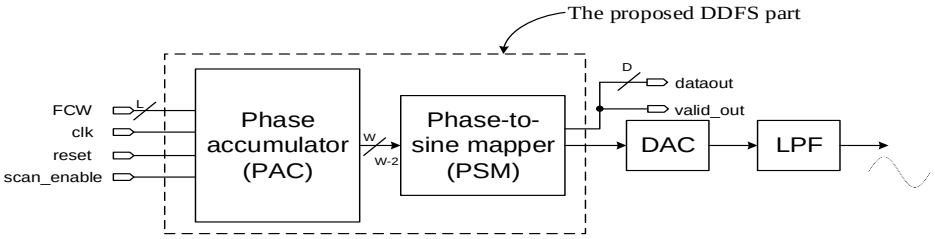

Fig. 1 DDFS block diagram

Table 1 Definition of input, output signal

Signal	Definition
FCW	Frequency control word, which is the cumulative PAC step
clk	System clock
reset	System reset signal
scan_enable	Enable signal, the system to work properly when set 1
dataout	Output digital sine wave sequence
valid_out	Output valid flag

Under the control of the L-bit frequency control word (FCW) and the reference clock (clk), the PAC generates a L-bit digital linear phase sequence and then undergoes sine-wave phase-amplitude conversion through the PSM to generate a discrete sequence of sinusoidal wave forms. It is then converted to an analog waveform by a digital-to-analog converter (DAC) and finally smoothed by a low-pass filter (LPF). This is the basic working principle of DDFS.

3. Quasi-linear interpolation algorithm

Because the sine wave symmetry for the ideal sine curve, in the range $[0,\pi/2]$, the closer to 0 closer to a straight line. Curves throughout the range can be fitted piece-wise by linear functions and polynomials. Through the analysis, it is found that in the range $[0,\pi/2]$, the boundary between the linear and parabolic polynomial segments is $3/4$ [2], that is, in the range $[0,\pi/8]$ of linear segment, the

segment is fitted by the linear equation $y_i = a_i x + c_i$ while the range $[\pi/8, \pi/2]$ is fitted by the parabola equation $y_i = a_i x^2 + b_i x + c_i$, as shown in Fig. 2. The advantage of this method is that the computational complexity is lower than that of pure parabolic interpolation, and the accuracy of the approximate precision is higher than the linear interpolation [4].

The core of the piece-wise linear interpolation is the determination of the polynomial interpolation method, which determines the error of fitting the sine wave with respect to the standard sine wave and thus affects the spectral purity of the output [5]. Algorithm research should take into account the complexity of the calculation and spectral purity. The basic interpolation method includes linear interpolation method, parabola interpolation method and linear interpolation method [2]. There are two kinds of segmentation methods: uniform and non-uniform [4] [5].

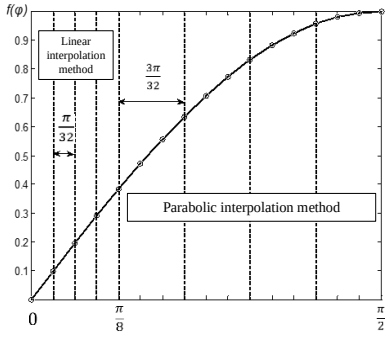

Fig. 2 Quasi-linear interpolation

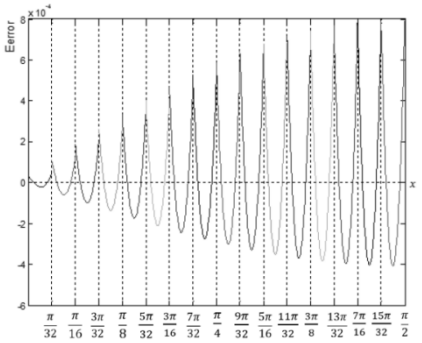

Fig.3 Linear interpolation error curve of 16 average segments

According to the literature [4], we can see that the sinusoidal wave with good spectral purity can be obtained when the 16 segments are evenly divided by piece-wise linear interpolation, which is about 90dBc. As a reference, with MATLAB fitting, we can finalize the DDFS design of this cutting method. We know that under different splitting conditions, the error between the fitted sine wave and the ideal sine wave is different, and the size of the error value determines the spectral purity of the output sine wave. It can be seen from Figure 3, there is a certain error between the fitted sine wave and the standard sine wave.

In order to determine our segmentation method, we first fit the sine wave by dividing the 16 segments in the literature [4], and get the curve of the error under this segmentation method, as shown in Fig.3.

As can be seen from Fig. 3, when using the linear interpolation method to divide the sine wave into a 16-hour average, the maximum error between the fitted waveform and the ideal sine wave is approximately 8×10^{-4}. Taking this value as a reference, the linear interpolation method is used to fit the sine wave. After MATLAB fitting, the final determination of this DDFS design cutting method. That is divided into 4 sections in the section $[0, \pi/8]$, using linear interpolation method, the interval is $\pi/32$; $[\pi/8, \pi/2]$ section is divided into 4 sections, using parabolic interpolation method, the interval is $3\pi/32$. As shown in Fig. 4:

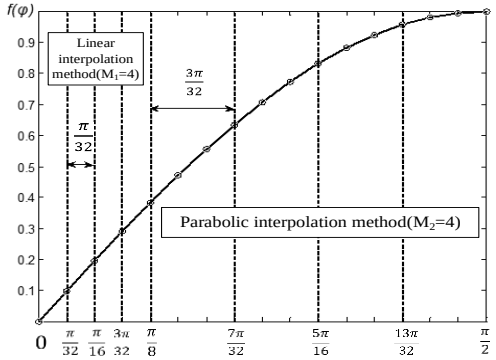

Fig. 4 This proposed quasi-linear interpolation

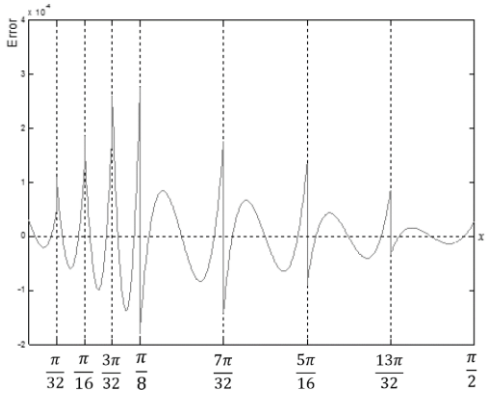

Fig. 5 The proposed interpolation error curve

In other words, using quasi-linear interpolation method, we can cut the 8 segments can be compared to the linear interpolation method to cut 16 segments is also close to the ideal sine wave waveform. And based on the above interpolation sine wave and ideal sine wave error curve shown in Fig. 5.

It can be seen from Fig. 5 that the maximum error is $\pi/8$, and that the error between the fitted sine wave and the ideal sine wave using the above linear interpolation method is much smaller. Table 2 shows the approximate polynomial coefficients of each segment.

Table 2 Approximations of polynomial coefficients in each sub-section

Coefficients	ai	bi	ci
1	0.9985	-	0.0000
2	0.9889	-	0.0010
3	0.9698	-	0.0049
4	0.9413	-	0.0133
5	-0.2566	1.1330	-0.0228
6	-0.3699	1.2874	-0.0758
7	-0.4513	1.4456	-0.1529
8	-0.4938	1.5523	-0.2199

4. Design of DDFS Circuit Based on Linear Interpolation Method

In a DDFS system, DACs and LPFs are implemented by existing devices, and the PAC and PSM sections are designed in this paper.

PAC is the most basic part of DDFS and consists of an L-bit adder and an L-bit register cascaded. Under the action of the clock clk, the FCW is added in steps, generating a full-scale overflow [4].

PSM is the core part of DDFS. The traditional PSM module uses ROM look-up table to realize the sine amplitude corresponding to the phase of sinusoidal waveform stored in ROM. Under clock control, the phase sequence of PAC output is addressed to obtain the corresponding amplitude Value Sequence [9]. However, the capacity of ROM increases exponentially with the increase of PAC bit width [7]. Integrating such a large capacity ROM on a DDFS chip can increase the power consumption of the chip, increase the chip area, and slow down the operation speed [9]. This paper does not use ROM DDFS structure linear interpolation algorithm [5], instead of ROM memory-based look-up table, the phase of the sine wave amplitude conversion, in order to achieve the need to reduce hardware costs [5].

According to the symmetry of the sine wave, the first quadrant waveform can be inverted symmetrically to obtain a complete sine wave. Therefore, two complementers are used in the circuit to achieve waveform symmetry inversion. In this design, with the most significant bit (MSB1) and second most significant bit (MSB2) as the symmetrical flip control bit. Therefore, this part of the design of the DDFS block diagram shown in Fig. 6. Phase-to-sine amplitude converter for sine phase-amplitude conversion module.

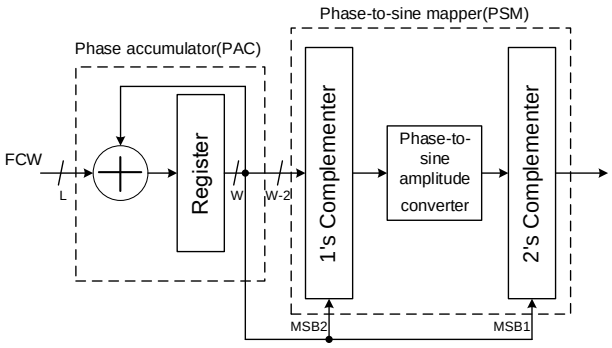

Fig. 6 The proposed DDFS block diagram

In the design of DDFS, the phase truncation technique is usually used. That is, the high W bit of the PAC output is taken as the input of the PSM, which can greatly reduce the computational complexity of the PSM part and have little effect on the spectral purity of the output sine wave , That is, in Fig. 6, L> W.

In the circuit structure part of the phase-to-sine amplitude converter, according to the discussion of the algorithm above, there is a multiplication and square operation in the design, and the multiplication of the multiplier can slow the speed of the circuit , So we consider using shifters and adders instead of very large multipliers. When the equation $y_i = a_i x^2 + b_i x + c_i$ of the circuit is implemented, taking into account the form rewritten into $y_i = a_i (x + b_i)^2 + c_i$ can reduce the multiplication, we will make the above coefficients changed accordingly. At the same time, the first 3 ~ 5 high MSB3, MSB4, MSB5 used to control the timing of the operation. Therefore, the design PSM part of the circuit structure shown in Fig. 7:

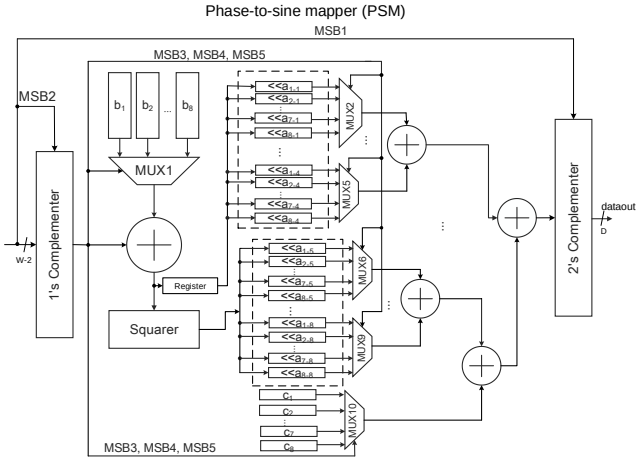

Fig. 7 PSM circuit structure

5. FPGA implementation

FPGA is a good choice for high-speed, high-performance digital devices. This article uses FPGA to design DDFS. In this design, the input FCW is L = 32 bits, the output bit D = 18 bits. Therefore, the PAC bit width is 32 bits, which uses a 32-bit register, 32-bit adder. DAC is a ready-made resource on the FPGA development board.

5.1 DDFS FPGA implementation

Write the corresponding Verilog code according to the designed circuit structure and then download it to the FPGA board to run. The PFGA development board model used is Altera Corporation Cyclone II EP2C35F672C6. After power-on reset, connect the output terminal to the oscilloscope to observe the experimental environment and The result is shown in Fig. 8. From the oscilloscope, we can see the full sine wave output.

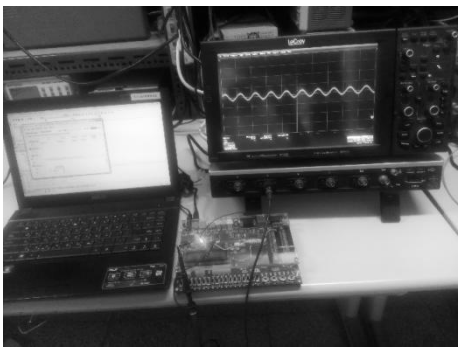

Fig. 8 DDFS FPGA implementation

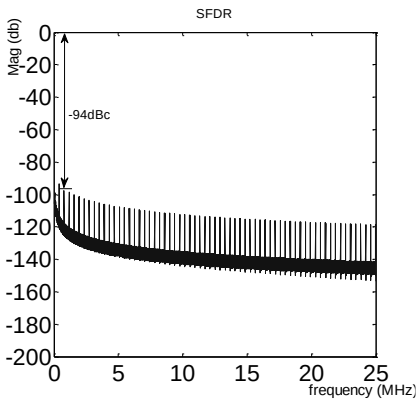

Fig. 9 SFDR

5.2 DDFS performance parameters

5.2.1 Frequency resolution Δf0

$$\Delta f_0 = \frac{f_c}{2^N} \tag{1}$$

In (1), f_c is the system clock signal frequency, FPGA board crystal 50M, so f_c = 50M, N is the phase accumulator word length, the design of N = 32, the above formula available, the design of the DDFS frequency The resolution Δf_o is 7.45e-7Hz.

5.2.2 Output sine wave frequency f0

$$f_0 = \frac{FCW}{2^N} f_c \tag{2}$$

It can be seen from the above formula, the output frequency and frequency control word FCW is proportional. The maximum output frequency is limited by the Nyquist sampling rate, so $f_0(\max) = 1/2\, f_c$.

5.2.3 Spurious-free dynamic range (SFDR)

The SFDR after the truncation of the DDFS phase is given by the following equation[10]:

$$SFDR = 20\log_{10}\left(\frac{\sin\frac{\pi(2^W-1)}{2^N}}{\sin(\frac{\pi}{2^N})}\right)dBc \tag{3}$$

In equation (3), W is the phase accumulator output phase truncated word length, the design, W = 20, which can be calculated, SFDR = 120dBc However, due to the nonlinear DAC and other factors, making SFDR value is generally less than the theoretical value, the sine wave spectrum analysis by FFT transform, SFDR and frequency curve can be obtained, shown in Fig. 9, the analysis shows that this design SFDR value up to -94dBc.

6. Conclusion

In this paper, the polynomial interpolation of the phase-to-amplitude conversion module (PAC) in DDFS is analyzed, and the linear interpolation algorithm and the method of segment-specific segmentation are proposed. The FGGA is implemented on Altera's Cyclone II device. Based on this algorithm, DDFS achieves better performance in terms of frequency resolution, SFDR, working frequency and so on. In particular, the frequency resolution Δfo reaches 7.45e-7Hz and the SFDR value reaches -94dBc, thus achieving high precision, High spectral purity sine wave output. In addition, if an LPF is connected to the DAC and the sine waveform is smoothed out, the spectral purity can be further improved.

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