Geiger-Mode APD Single Photon Detectors

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Abstract

Avalanche photodiodes (APDs) operating in Geiger mode can detect weak optical signals at high speed. The implementation of APD systems in a CMOS technology makes it possible to integrate the photodetector and its peripheral circuits on the same chip. In this paper, we have designed SPAD in a commercial 0.18-μm CMOS technology. The APD are theoretically analyzed, calculated, simulated and the results are interpreted. Excellent breakdown performance is simulated for the 20μm APDs at 22.0V. The SPAD device is compared to the previous implementations in standard CMOS. Our APD has a 55% peak photon detection efficiency (PDE) at an excess bias of 2V, and a 3.2kHz dark count rate (DCR), which is better than the previously reported results.

Keywords

Avalanche photodiodes (APDs), breakdown performance, photon detection efficiency (PDE), dark count rate (DCR).

1. Introduction

CMOS single-photon avalanche diode (SPAD) based imagers are being increasingly adopted in applications ranging from microscopy[1-2] to biological diagnostics[3-4] to space telescopes[5] to consumer electronics[6]. As the application field expands, the need to enhance SPAD performance, and especially photon detection efficiency, is also increasing. In CMOS technology, SPAD design is not only limited to the available implant/diffusion layers but it is also constrained by the need of circuit integration, so as to enable larger monolithic arrays. In this work we focus on realizing high performance CMOS SPADs that, at the same time, facilitate circuit integration.

In this work we report a substrate isolated SPAD, designed using narrower depletion junction with a relatively wider photon collection region. The SPAD designed in 180nm CMOS technology achieves photon detection efficiency can be theoretically enhanced either by designing the main junction with a wide depletion region or by widening the region where photo-carrier diffusion takes place. In case of wide depletion, an excess bias higher than 10V is required to enhance avalanche triggering probability[7]. In case of a widened of photo-carrier diffusion region, high sensitivity can be achieved with a relatively narrow depletion region and thus a lower excess bias. However, a drawback of the photo-carrier diffusion process is a long exponential tail in the time response of the SPAD[8]. CMOS SPADs[9-10] designed using substrate as photon collection region have led to the realization of high photon detection efficiency.

The remainder of the paper is organized as follows: Section II describes the device design. Section III presents simulation results along with the state-of-the-art comparison. Section IV concludes the paper.

2. The SPAD device design

The p-n diode is realized using a P+/n-well/DNW/P-sub junction (see Fig. 1) in the 180-nm CMOS technology. In this design, p+ functions act as anode and n-well acts as cathode. In this construction, DNW/P-sub assures substrate isolation, while DNW provides a contact to n-well. In contrast to where

a virtual guard ring is realized, in the presented design, premature edge breakdown is avoided utilizing p-well lateral diffusion and a lightly doped n-well around it.

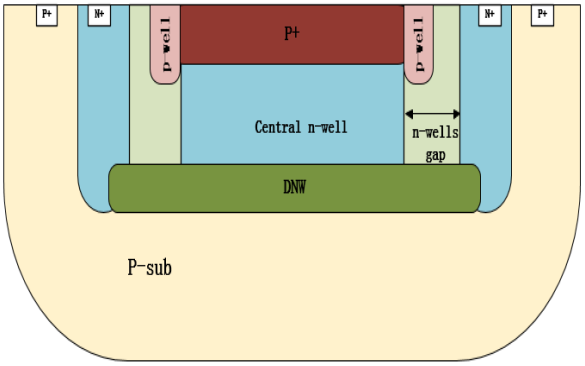

Fig. 1 The designed SPAD structure

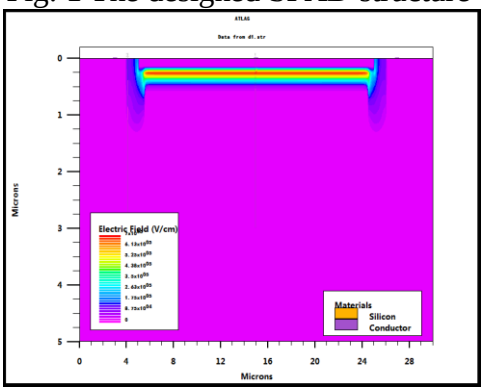

Fig. 2 The electric field distribution

A field profile of this device is shown in Fig. 2. In this case, the combination of the two types of implants forms a guard ring, lower filed strength at the edges than central pn junction. More details can be described in Fig. 3 and Fig. 4.

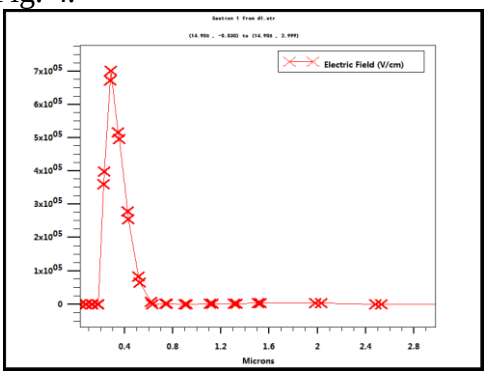

Fig. 3 Central pn junction longitudinal electric field distribution

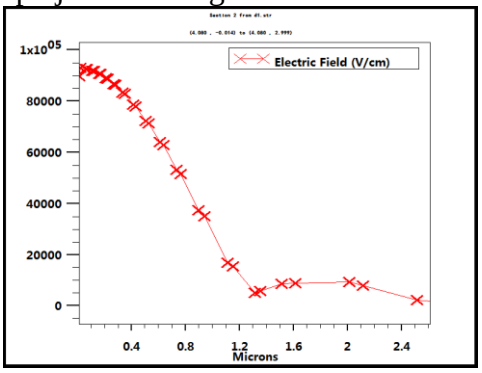

Fig. 4 Edge pn junction longitudinal electric field distribution

Breakdown will occur in the regions of highest field strength the interface of the strongly doped materials. In this structure, it occurs naturally in a planar region where the increasing oping concentration of the p+ layer meets the central n-well, in the depth range from 0.25um to 0.5um(see Fig. 3). Around the periphery of the SPAD, the reduced doping concentration of the p-well toward the surface will result a wider depletion region and lower field strength inhibiting breakdown(see Fig. 4).

3. I-V characteristics and multiplication factor

The simulation result of the breakdown voltage, see Fig. 5. To determine where the actual breakdown spot was, we used a novel simulation method, which is using the current density simulation results at the breakdown voltage to find the breakdown current flow path.

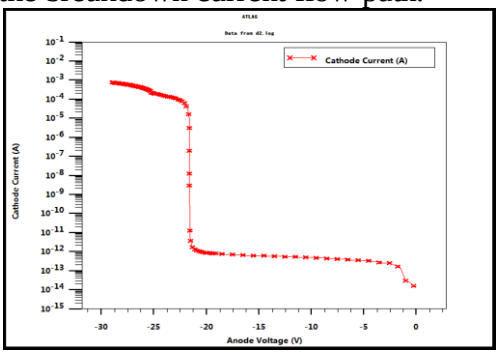

Fig. 5 I-V characteristics curve

In Fig. 5, I was found to slowly increase until VBD was reached at excess bias voltage, Ve = 21.3 V, and then rapidly increase due to avalanche multiplication.

Using the following relationship, a light source with 600nm wavelength and 100nW optical power in order to calculate the the photocurrent gain, as show in Fig. 6 as a function of reverse bias, could be calculated:

$$\text{gain} = \frac{I_{\text{ph}} - I_d}{I_{ph0} - I_{d0}} \tag{1}$$

Maximal gain up to 1e6 when excess bias voltage is 8V in p-sub GR SPAD. The SPADs high internal gain make sure that they can detect fairly low intense light.

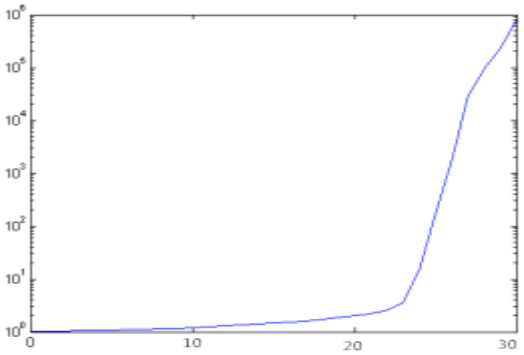

Fig. 6 Gain factor curve

4. Photon detection efficiency versus dark count rate trade-off

The PDE is a definition of the ratio of the number of detected photons to the number of incident photons[11]. It is the product of the geometric fill-factor, absorption probability, and triggering probability. Technology parameters play a significant role in determining PDE. For an impinging photon to be detected by an SPAD fabricated in standard CMOS technology. first, the impinging photon must pass through a thick layer of passivation that is put on top of the chip at the end of the process to protect it from external contaminants. Then, the light must pass through several layers with different refractive induces, possibly undergoing constructive and destructive interference in the

insulating films directly above the active silicon surface. Custom CMOS imaging technology facilitates optimization of the dielectric above the active region to minimize reflections, but standard technologies do not offer such options. Therefore, post-processing may be used to etch the top passivation layers, and this leads to a marked improvement in performance. Once the photon reaches the silicon surface, it must be able to strike the photosensive area of the detector. Typically, this is achieved by optimizing the SPAD guard-ring ring structure, reducing the transistors dimensions with technology down scaling, reduction of in-pixel transistor count and utilization of n-well sharing among SPADs. Typically, the incident photon must be absorbed in the depletion region of the SPAD to trigger Geiger pulses. Also, photons absorbed within a few diffusion lengths of the depletion region edges in the quasi-neutral regions can potentially trigger Geiger pulses if the photo-generated minority carriers diffuse into the depletion region.

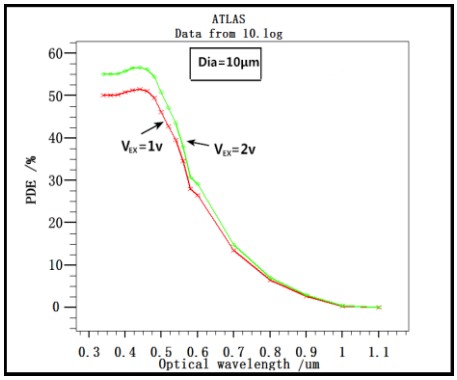

Fig. 7 PDE in different excess voltage

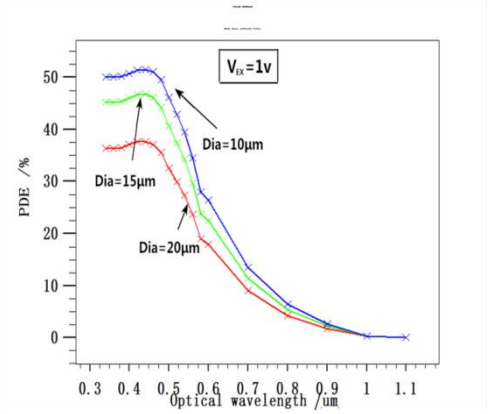

Fig. 8 PDE in different diameter

SPADs in standard CMOS technology can made from shallow junctions or deeper junctions depending on the design options available. Deeper in the substrate, photons with longer wave-lengths are more likely to be absorbed. Thus deeper junctions are more sensitive to longer wavelengths as compared to shallow junctions close to the semiconductor surface. So SPADs designed in CMOS technologies with shallow active regions favor the detection of photons absorbed near the silicon surface, resulting in a PDE response suitable for near UV-blue incident light. Since the shallow-junction SPADs have thinner active regions due to the high doping concentrations used, their PDE is smaller than the p-well/deep n-well junction SPAD over the excess voltage range. Fig. 7and Fig. 8 illustrates the trend of PDE of several different SPADs in diameter and excess voltage. As the absorption depth in silicon begins to drastically increase for wavelengths beyond 400 nm, then the SPAD is rendered transparent to blue light.

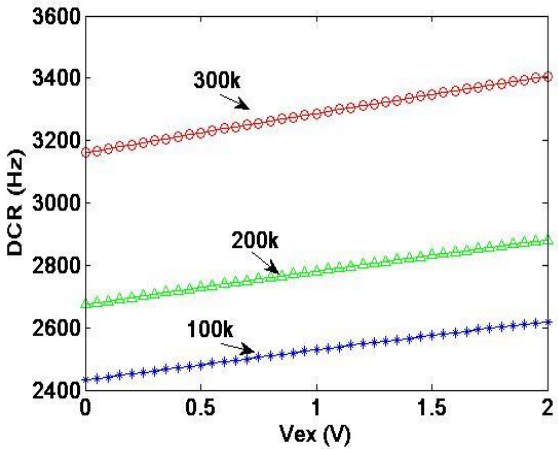

Fig. 9 DCR in different temperature

Fig. 9 shows the DCR under different excess bias. It is observed that the DCR keeps rising exponentially as the excess bias increases. In our SPAD, a DCR of 3295 cps was simulated at 1 V excess bias. In general, in wide depletion devices, lower tunneling noise is expected. Above 1 V of

excess bias, DCR is more dependent on voltage than on temperature, suggesting that a major contributor to noise is tunneling. We believe that a higher tunneling contribution is due to the exposure of P+ edge to high electric field that resulted from widening the depletion region due to increased excess bias.

5. Conclusion

Summary of the performance of the proposed SPAD implemented in different CMOS technology is shown in Table 1. VBD means the breakdown voltage, Vex means the excess bias.

Table 1 Comparation of main characters in SPADs

Ref.	Process	VBD/V	DCR/Hz	PDE/%@Vex
This SPAD	0.18 CMOS	22	5-6K	51@2
Ref.12	0.35 CMOS	13	<1K	5@3
Ref.13	0.18 CMOS	10.8	-	23@1
Ref.14	0.18 CMOS	26	<1K	50@6
Ref.15	0.18 CMOS	12	1K	15@1

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