# Design of A 60 GHz Power Amplifier utilizing 90nm CMOS Technology

Wei Wang [1, a], Mengjia Huang [1, b] and Yongchun He [1, c]

Chongqing University of Post and Telecommunications, Chongqing 400065,P.R.China;.

[a]260969133@qq.com, [b]Ybxhmj@126.com, [c]1149443231@qq.com

## Abstract

**In order to satisfy the short-distance high-speed wireless transmission communication system, such as Wireless Personal Area Net-work (WPAN) applications. A 60GHz high efficiency single ended power amplifier is proposed, which is with three stages cascade structure, and it is design with SMIC 90nm 1P9M CMOS technology. The on-chip spiral inductor with small inductance and high-quality factor is designed with the top metal layer, this type of spiral inductor can be used as the passive circuit for input, output and inter-stage impedance matching network circuits design in order to improve the overall performance of the PA. The additional power efficiency will be increased by the reduction of the transmission losses and output matching losses. The simulation results show that the power amplifier can achieve the power gain of 17.2dB, the output power is 8.1dBm at 1dB compression point, the saturated output power is 12.1dBm, the peak power additional efficiency is 15.7% and the DC power consumption is 70mw at 1.2 V voltage supply.**

## Keywords

**CMOS; Power Amplifier; three cascade structure; power additional efficiency.**

## 1. Introduction

In recent years, as demand for high data rates for short-range communications within 10 meters has been on the rise, unlicensed bands (59-64 GHz) driven by the 802.11ad and 802.15c standards are of worldwide concern. 60GHz technology with high data transmission capacity, high security, strong anti-interference ability [1]. CMOS technology is used in millimeter-wave front-end circuit design due to its low cost and high integration. The main challenge in integrating millimeter-wave communications using low-cost technology is to design a power amplifier (PA) that meets power requirements. However, the low breakdown voltage of CMOS devices greatly limits the output power. How to improve the power added efficiency (PAE) when the maximum output power is obtained is the biggest challenge to design a millimeter wave PA. Up to now, some well-behaved 60GHz CMOS power amplifiers [2-10] have been reported in the literature. The PAEs of PA are mostly below 12% at high gain or high output power. The research by P.H. Chiang et al. [8] shows that the saturation output power can be as high as 16dBm through multiple coupling, but the power gain and PAE are only 9.2dB and 7.2% respectively. Studies by Y.S. Lin et al. [9] obtained gains of up to 30 dB using a cascade of 5 stages, but with a PAE of only 9.7%.

In order to achieve sufficient power gain and output power at the same time get a higher PAE. This paper presents a 90nm CMOS process can be applied to 60GHz communication system of high efficiency three cascaded power amplifier. The first section of the article mainly introduces the power amplifier design considerations, to analyze the additional power efficiency; Section 2 introduces the circuit layout and simulation results; Section 3 gives the conclusion.

## 2. PA Circuit Design and Analysis

### 2.1 Overall design and analysis

The design of CMOS millimeter-wave power amplifiers is limited by the output voltage swing and low power gain due to low transconductance of the transistors. So its design needs to compromise between power gain, linearity and efficiency.

Key performance parameters that measure PA performance are analyzed from its FoM expression (1): FoM$_{PA}$ is proportional to the square of the output power (Pout), PAE, power gain (G), and frequency. The output power and gain will decrease with increasing frequency. Although the nMOSFETs exceed 8dB at 60GHz in a standard 90nm process library, they can dissipate 3-4dB in the matching network and at the same time, the input impedance matches up to 50Ω, which can also cause inductance degradation and limit gain. Literature [3-4] designed two cascaded structure, PA gain are less than 10dB. Therefore, this paper uses three cascaded structure, in order to obtain sufficient gain.

$$FoM_{PA} = P_{out} \times G \times PAE \times f^2 \tag{1}$$

Power amplifier power efficiency (PAE) is:

$$PAE = \frac{P_{out} - P_{in}}{P_{diss}} \times 100\% \tag{2}$$

Based on the load-pull theory, the maximum output power of the amplifier can be obtained by performing load impedance transformation on the output impedance of the amplifier:

$$P_{sat\,max} = 10\log(10^3 \times \frac{1}{2}|V_{load} \times I_{load}|) \tag{3}$$

The millimeter-wave band loss for the entire circuit will have a tremendous impact. So the value of the load drawn by the load is not the best load value, consider the loss of the output matching network will be saturated Output:

$$P_{sat50\Omega} = P_{sat\,max} - P_{match\_loss} \tag{4}$$

According to [11], the closer the output load value is to 50Ω, the smaller the output matching loss is. In this paper, by increasing the size of the power amplifier output stage transistor to increase its saturation output power to meet the system requirements and make the load impedance close to 50Ω, in order to minimize the matching loss and improve the power amplifier PAE. In fact, unlike low-frequency applications whose operating frequency is farther away from the transistor's maximum oscillation frequency (fmax), the output power of the device shows a quasi-logarithmic increase with increasing transistor size. At 60 GHz, the increase in device size also depends on the parasitic effects of the transistor, that is, the gate-to-source capacitance, the gate-to-drain capacitance, and the access resistance, which are compromised.

## 2.2 Small inductor design.

In 60GHz frequency band, the inductance value that the circuit design needs is very small, the range is between 50pH and 200pH. Inductance of on-chip spiral inductor provided in CMOS technology library is too large and self-resonant frequency is less than 60 GHz, which does not meet the circuit design requirements. The published 60GHz power amplifiers, most of them using the simple structure, easy to model the transmission lines (such as microstrip line [4], coplanar waveguide [5], grounded coplanar waveguide [3]) to achieve small inductance function. However, for a given inductance, the use of an on-chip spiral inductor can effectively improve the quality factor, Q, and on-chip spiral inductors can greatly reduce the area of passive components relative to the transmission line.

This paper proposes the design of spiral inductors using metal_9. HFSS 13.0 modeling and electromagnetic field simulation analysis, which can be used for Cadence layout design of small inductance. An inductor model that meets the PA circuit design requirements is shown in Fig. 1, with an internal diameter of 25μm, a linewidth of 5μm, an equivalent inductance of 110pH and a quality factor Q of 21. The area is only 42μm×42μm.
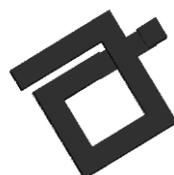


Fig. 1 Uses the top metal design of the inductor

## 2.3 Core circuit design

In this paper, all the circuits of the power amplifier are biased in Class A, and the first stage adopts a Cascode structure with adaptive bias (with inductive negative feedback). This is to improve the gate oxide breakdown problem, but also reduces the hot carrier effect and increases the reliability and lifetime of the device. At the same time using Cascode structure can get higher gain, better reverse isolation, reduce Miller effect, taking into account the input / output matching. Both the second and third stages are common-source topologies for better linearity and higher efficiency at low supply voltages. Circuit structure shown in Fig. 2.
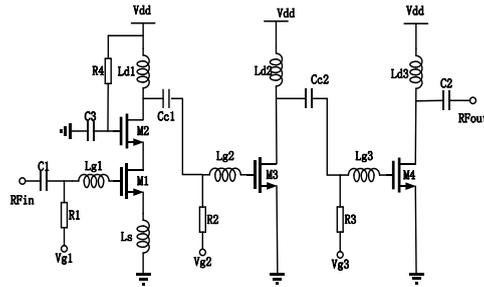


Fig. 2 60GHz power amplifier circuit

According to[3], when the transistor drain current density is 0.15mA/μm, 0.2mA/μm and 0.3mA/μm, they correspond to the minimum noise figure, the maximum power gain and the optimal linearity, respectively. Therefore, the first-level transistor current density is biased at 0.2 mA / μm to obtain the maximum power gain, and the second-level and third-level transistor current densities are biased to 0.28 mA / μm to obtain sufficient linearity. The common-source transistor is biased by an external bias, for which a high-value resistor (5kΩ) is placed between the gate and the bias. The proposed PA is designed to operate at a 1.2V supply voltage. According to IEEE 802.15.c (TG3c) and the Wireless HD Working Group recommendations, transmitters for 60GHz communications need to provide 10dBm transmit power into the antenna to meet electromagnetic field emission Global requirements. According to the load line theory:

$$P_{\max} = \frac{I_{DC} \times (V_{DD} - V_{ds,\,sat})}{2} \tag{5}$$

$I_{swing} = (0.4\text{m}A/\mu\text{m}) \times W$ as the 1dB compression point before the maximum swing current, instead of $2 \times I_{DC}$ available P1dB:

$$P_{1dB} = \frac{I_{swing} \times (V_{DD} - V_{ds,\,sat})}{4} \tag{6}$$

It can be drawn transistor size (W) and bias current density as:

$$W = \frac{4 \times P_{1dB}}{\left[ (0.4\text{m}A/\mu\text{m}) \times (V_{DD} - V_{ds,\,sat}) \right]} = I_{DC}/(0.3\text{m}A/\mu\text{m}) \tag{7}$$

Among them $V_{ds,\,Sat} \approx 0.3$V, according to the bias current density is the output stage MOS tube size 22.2mA/(0.28mA/um)≈80um, so the output stage MOS tube M4 size is set to 40×2um. The best distribution of the power gain and bias current between levels, both of which will determine P1dB, can be derived from the linearity derivation in the cascaded system, equation (8).

$$\frac{1}{OP_{1dB,\,cascade}} = \frac{1}{OP_{1dB3}} + \frac{1}{OP_{1dB2} \times G_3} + \frac{1}{OP_{1dB1} \times G_2 \times G_3} \tag{8}$$

Therefore, the transistor sizes of the first and second stages are respectively 32×2μm (M1, M2) and 36×2μm (M3) according to the formula (8).

The input matching consists of a source degeneration inductance Ls and a gate inductance Lg1. The source inductance Ls matches the real part of the input impedance to 50 Ω and the gate inductance Lg1 cancels the imaginary part of the input impedance. At the output using a load inductor Ld3 and capacitor C2 form a L-type matching network, the most simplified output matching to reduce the matching loss. Inter-level matching are first-level L-type matching networks. The pre-stage output and post-stage input are both impedance matched conjugate matched for maximizing power transfer, and the second and third stages eliminate the source negative feedback Inductance to increase the amplifier gain. While matching is narrow-band matching, the simplicity of matching networks is particularly important for minimizing series-parasitics and its effects are particularly noticeable in millimeter-wave bands.

## 3. Layout Design and Simulation Analysis

### 3.1 Layout design

In this paper, PA SMIC 90nm 1P9M RF CMOS process, complete the layout design in Cadence virtuoso platform. The spiral inductors used in the layout are all geometric parameters given by HFSS for electromagnetic field simulation. Capacitors use MIM capacitors with a capacitance of 1.0 fF / um2. In layout design, in order to reduce the parasitic capacitance, coupling and other losses caused by the power line as much as possible to use a thick top metal (thickness of 3μm) alignment, while reducing the layout area as much as possible to reduce the alignment Length, input and output to maintain the farthest, left into the right out. Layout shown in Fig. 3, the area (400μm × 300μm).
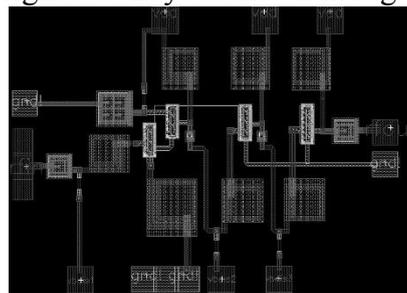


Fig. 3 Layout of the 60 GHz PA

### 3.2 Post-simulation analysis

Use Cadence Specter (RF) to simulate your layout by continually optimizing your layout. Power supply voltage is the standard process voltage of 1.2V, all levels of bias voltage Vg from front to back were 0.8V, 0.85V and 0.89V. Fig. 4 to 5 shows the power amplifier S-parameter simulation and stability factor Kf simulation diagram. The gain S21 of the amplifier is 17.2dB at the operating frequency of 60GHz, which shows that the cascaded cascade structure with Cascode as the gain drive stage improves the circuit gain very well and achieves a high amplification of small signal to satisfy 60GHz ultra-short distance communication system requirements. The input / output matching measures S11 and S22 are both less than -10 dB, indicating good circuit matching. Stability factor Kf is greater than 1, the circuit is absolutely stable.
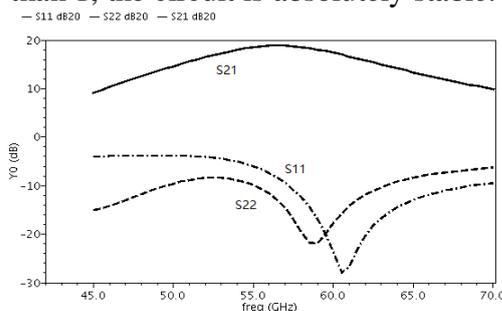


Fig. 4 S-parameter simulation                    Fig. 5 Stability factor K
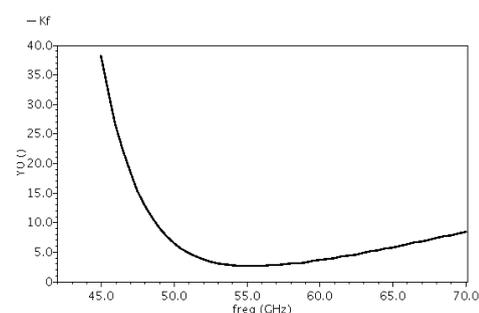
Fig. 6 to 8 depicts the PA operating frequency of 60GHz case of large signal performance increases with the input power curve. The results show that the power gain is more than 17dB and the gain

curve is flat. The output power (OP1dB) at the 1dB compression point is 8.1dBm, the saturated output power (Psat) is 12.1dBm, and the power added efficiency (PAE) peak is 15.7%.
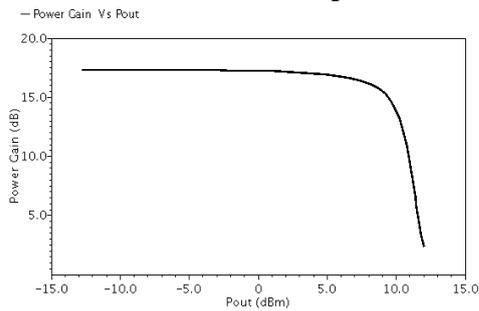


Fig. 6 Power gain curve                    Fig. 7 1dB compression point output power curve
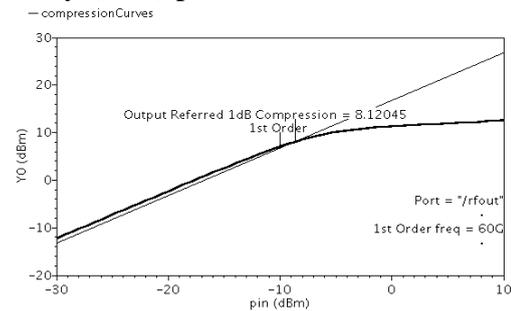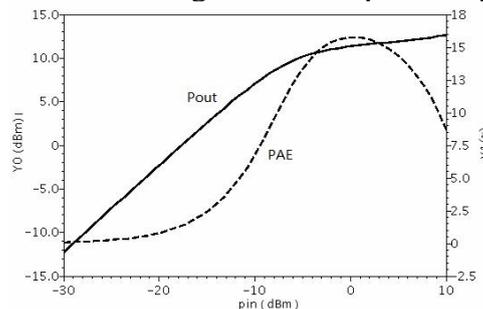


Fig. 8 Output power and power added efficiency curve

## 4.   Conclusion

Based on the SMIC 90nm CMOS process, this paper presents a three-stage cascaded power amplifier with operating voltage of 1.2V applied in the 60GHz frequency band. By analyzing the output loss and device size, etc., the power added efficiency is improved. The cascode and common source structure are used to improve the circuit gain. The electromagnetic inductance of the spiral inductor on the small inductance chip is designed to improve the overall performance of the circuit. Layout area of 400μm × 300μm, saturated output power of 12.1dBm, gain of 17.2dB, additional power efficiency of 15.7%, the overall performance is good, to 60GHz short-range wireless communication system requirements.

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