Doherty Power Amplifier with Extended Back-Off Range by Using Two-Section Quarter-Wave Transformer

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Abstract

In this paper, a Doherty power amplifier (DPA) using two-section quarter-wave transformer is proposed for broadband operation and extended power back-off range. The two-section quarter-wave transformer is used for main transformation and power combination. Its characteristic impedances are designed according to the maximally flat response theory and corresponding back-off impedance transformation ratio for wider power back-off range. The comparison between conventional transformer and proposed transformer shows that the broader impedance matching bandwidth can be achieved with the help of maximally flat response of proposed transformer. In addition, a band-pass network designed by two-point matching technique is used to realize broadband auxiliary impedance matching and load modulation. For verification, a Doherty power amplifier based on two commercially available gallium nitride HEMT (Cree CGH 40010F) devices was designed, fabricated and measured. Under the drive of continuous wave (CW) signal, the DPA has a 10-dB back-off efficiency of 30%-40% and a saturated efficiency of 48%-71% within the frequency band from 1.1 GHz to 1.6 GHz.Keywords

Keywords

Doherty power amplifier, broadband, back-off range, two-section quarter-wave transformer.

1. Introduction

The demand of high data rate and crowded spectrum in modern communication system require spectral efficient modulation schemes. That results in transmitting signal with large peak to average power ratio (PAPR). So the power amplifier (PA) should work at output power back off (OPBO) to sustain the linearity of amplification. But in the single PAs, high efficiencies can only be obtained at saturation, and the efficiencies degrade seriously at output power back-off. Now, the Doherty power amplifiers (DPA) which can provide high efficiency at back-off power are widely applied in industry. In addition, the broadband operation of PA is need in a lot of applications. It is necessary for PA to support the signals in different frequencies. However, the conventional DPA using a narrow $\lambda/4$ impedance transformer has the disadvantage of narrow bandwidth performance. In recent years, so many bandwidth enhancement techniques for DPA have been presented to overcome this problem. Some approaches can effectively extend the DPA's bandwidth and achieve high efficiency, like using different output structures [3]-[7], and controlling the output current or voltage ratio of main and auxiliary devices [3][7][9]. Those DPA cases can achieve high efficiencies at 6 dB back-off power and saturation in a wide bandwidth.

The efficient digital modulation schemes with higher PAPR have been adopted in modern wireless communication systems. Such as wideband code-division multiple access (WCDMA), it has a PAPR of 9.6 dB. That requires the DPAs to have high efficiency at larger back-off range. Most DPA works focus on 6 dB power back-off, which are not optimum for communication signals with PAPR around 10 dB. The researches of broadband high-efficiency DPAs are demanded. In [9], the power back-off point can be reconfigured by changing the main amplifier drain bias. If the drain bias voltage of main amplifier is reduced, the power back-off point of DPA can be early. Furthermore, to sustain the maximum output power and high efficiency at saturation, [9] also derive the output currents relations between main amplifier and auxiliary amplifier. Tuning the drain bias voltage of main device is a effective way to change the back-off range of DPA, but it need precise control of the two devices' output current, which is difficult to achieve. [9] achieves that by using two RF inputs, but it is not a convenient way. The [11] also proposes a DPA with output power back-off around 9 dB. It sustains the load modulation by controlling the ratio between the two branch currents that flow into the common load. [10] designs a DPA with 10 dB back-off range by utilizing the harmonic injection which is a novel technique. It has 10 dB power back-off efficiency about 46% and saturated efficiency about 78% -83% in the frequency band of 1.6GHz – 1.9GHz. In [7], a two-section λ/4 transformer is used to achieve broadband operation. The characteristic impedances of the λ/4 transmission lines are calculated by maximum flat response theory. According to the maximum flat response theory, the transformed impedances only have a little variation in a broad bandwidth. So when adopted as the main transformer, the two-section λ/4 transformer can realize broad back-off impedance matching. The [7] also deduces the relation between output currents of main device and auxiliary device so as to achieve better load modulation in broader bandwidth. In this paper, the two-section λ/4 transformer with maximum flat response is also used in the main device. But it is designed to achieve 10 dB back-off range. Because of its broadband feature, the DPA can realize broadband impedance matching at back-off power. In addition, the output matching of auxiliary device which is relative to load modulation at peak can't be neglected. So a band-pass type auxiliary transformer is added into the DPA to achieve broadband output matching of auxiliary device and load modulation. With extended back-off range, the proposed DPA can also provide considerable performance in a wide bandwidth.

The organization of this paper is as following. The detailed analyses of the two-section λ/4 transformer and load modulation are described in Section II. Section III is the statement of the DPA's circuit design. The simulation results and measurement results are given in Section IV. Conclusions are in Section V.

2. Analysis of Main Transformer

The main transformer is essential to back-off impedance transformation and load modulation. In this DPA design, we use two-section $\lambda/4$ impedance transformer as the main transformer. The diagram of load modulation of the proposed DPA is depicted in Fig. 1. At central frequency f_0, the main transformer is two lossless quarter-wave transmission lines with characteristic impedances Z_1 and Z_2. I_M and I_A are the output currents of main device and auxiliary device. The characteristic impedances Z_1 and Z_2 can be defined as

$$Z_1 = \sigma_1 R_0 \tag{1}$$

$$Z_2 = \sigma_2 R_0 \tag{2}$$

where R_0 is system impedance (generally be 50Ω). To achieve maximum efficiency at back-off, we should choose suitable σ_1, σ_2 to let the load impedance seen by main device fulfill

$$Z_M = \frac{R_{opt}}{\xi_b} = \alpha R_0 \tag{3}$$

R_{opt} is the optimal load impedance of main device. It satisfies the following condition

$$R_{opt} = \frac{V_{ds}}{I_{M,max}} = \beta R_0 \tag{4}$$

V_{ds} and $I_{M,max}$ represent the drain bias voltage and maximum output current of main device respectively. ξ_b ($0<\xi_b<1$) represents the power back-off point, at which the auxiliary device begins to

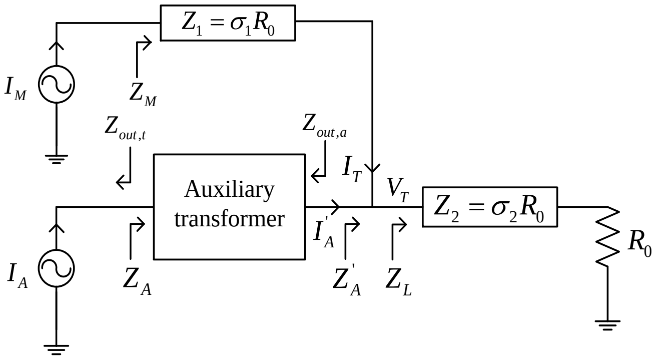


Fig. 1. Schematic of proposed DPA.

turn on. For simple analysis, we introduce variables α, β to denote the target impedances. According to (3) and (4), ξ_b fulfills

$$\xi_b=\beta/\alpha \tag{5}$$

Based on the transmission line theory, the load impedance at the power combination point is

$$Z_L=Z_2\frac{R_0+jZ_2\tan\theta}{Z_2+jR_0\tan\theta} \tag{6}$$

θ is electrical length of transmission line and it is 90° at f_0. Z_M can be transformed into

$$Z_M=Z_1\frac{Z_L+jZ_1\tan\theta}{Z_1+jZ_L\tan\theta} \tag{7}$$

Combining (1), (2), (3), (6), (7) at f_0, we get

$$\frac{\sigma_2}{\sigma_1}=\sqrt{\frac{1}{\alpha}} \tag{8}$$

So there are a continuum of pairs (σ_1, σ_2) that can fulfill (8). It has been proved that the performance of DPA is affected by the pair of (σ_1, σ_2) significantly. It mainly affects the impedance matching's bandwidth of main device. We should choose suitable (σ_1, σ_2) to realize broadband impedance matching. In conventional Doherty amplifier case, it is

$$(\sigma_1,\sigma_2)=(1,\sqrt{\frac{1}{\alpha}}) \tag{9}$$

For wider bandwidth, we consider the maximally flat response case. Referring to [7], the optimal pair (σ_1, σ_2) is

$$(\sigma_1,\sigma_2)=(\sqrt{\frac{\alpha+\alpha\sqrt{\alpha}}{2}},\sqrt{\frac{1+\sqrt{\alpha}}{2}}) \tag{10}$$

To verify different cases' result of the proposed DPA, we should calculate α, which is relative to ξ_b. And ξ_b depends on the power back-off range. To determine ξ_b, we need to infer the output power of main and auxiliary device. That requires the derivation of their current ratio, voltage profiles and bias conditions. These derivations are based on the requirement of load modulation of Doherty operation. The Doherty operation usually requires the main device to sustain maximal drain voltage profile at peak power, so that the DPA can output large power and high efficiency at peak power. So the output current ratio between main and auxiliary device should be designed precisely. So many Doherty amplifier works refer to this in recent years. Especially [7], it gives out the analyses of generalized current profile and generalized voltage profile, which are helpful for DPA design. According to [7], the maximal current amplitude of auxiliary device $I_{A,max}'$ at f_0 can be deduced as

$$I_{A,max}'=\frac{\frac{\sigma_1^2}{\sigma_2^2}-\beta}{\sigma_1}I_{M,max}$$

$$=\frac{\alpha-\beta}{\sigma_1}I_{M,max} \tag{11}$$

The maximal voltage amplitude at power combination point is

$$V_{T,max}=\frac{\sigma_1}{\beta}V_{ds} \tag{12}$$

Then the maximal output power of main device $P_{M,max}$ and auxiliary device $P_{A,max}$ are

$$P_{M,max}=\frac{1}{2}I_{M,max}V_{ds} \tag{13}$$

$$P_{A,max}=\frac{1}{2}I'_{A,max}V_{T,max} \tag{14}$$

So the maximal output power of the proposed DPA is

$$\begin{aligned} P_{out,max}&=P_{M,max}+P_{A,max}\\ &=\frac{1}{2}(I_{M,max}V_{ds}+I'_{A,max}V_{T,max})\\ &=\frac{1}{2}(\frac{\alpha-\beta}{\beta}+1)I_{M,max}V_{ds} \end{aligned} \tag{15}$$

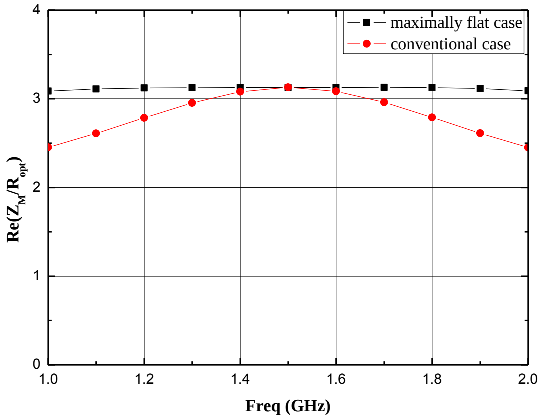
Considering $\xi_b=\beta/\alpha$ and the requirement of 10-dB power back-off range, we can calculate ξ_b by formula

$$10\lg(\frac{\xi_b P_{M,max}}{P_{out,max}})=-10\text{dB} \tag{16}$$

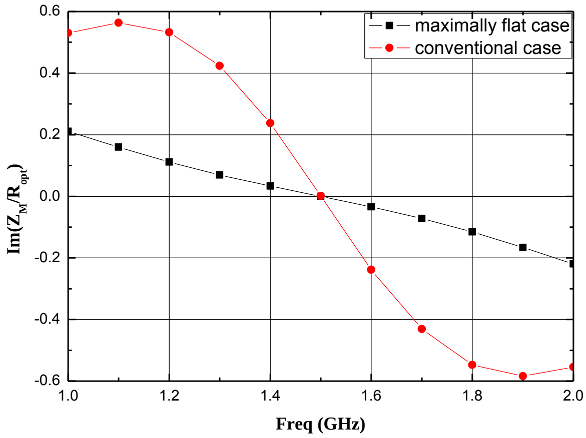
$$\frac{\xi_b P_{M,max}}{P_{out,max}}=\xi_b^2=0.1 \tag{17}$$

So ξ_b=0.32 is obtained. To obtain the parameter α, we also need to know the R_{opt} (parameter β). The optimal load impedance of main and auxiliary transistors can be obtained by load-pull simulation under the bias conditions at -3.0V and -5.8V. We choose the main transistor's optimal load impedance at f_0 (1.5 GHz) for analysis. Finally, β=0.4, α=1.25 and σ_1=1.15, σ_2=1.03 can be got from (4), (5) and (10).

The comparisons between conventional case and maximally flat response case of the two-section $\lambda/4$ transformer are shown in Fig.2 and Fig.3. The variations of real part and imaginary part of target impedances with different back-off impedance ratios (ξ_b=0.32, α=1.25 and ξ_b=0.5, α=0.8) are given out. These figures show that the two-section $\lambda/4$ transformer with maximally flat response can achieve wider impedance matching bandwidth compared to conventional case, regardless of what the impedance conversion ratio is. So the two-section $\lambda/4$ transformer with maximally flat response is used to achieve broadband back-off impedance matching in this design.

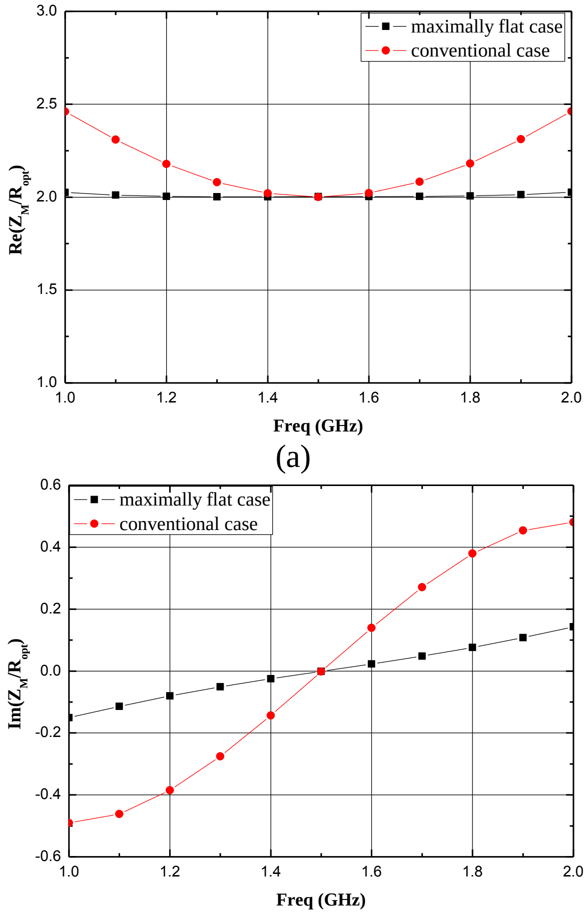


(a)



(b)

Fig. 2. Variations of impedances after transformations with ξ_b=0.32, α=1.25. (a)Real part. (b)Imaginary part.



(a)

(b)

Fig. 3. Variations of impedances after transformations with ξ_b=0.5, α=0.8. (a)Real part. (b)Imaginary part.

3. Design of Proposed Circuit

In section II, the main transformer in DPA and the back-off range of DPA are discussed. But the auxiliary branch of DPA is relative to maximum output power and load modulation. It can't be neglected in DPA's design. So in this work, an auxiliary transformer is utilized to realize better impedance matching, so that the DPA is able to have higher efficiency and power at saturation. In addition, the auxiliary transformer has impact on the auxiliary branch's output impedance, which affects the main load impedance at back-off. In general, the output impedance of the auxiliary transformer should satisfy quasi-open circuit condition. Besides realizing the impedance matching, the auxiliary transformer should also have minimal phase variation in the output reflection coefficient.

For above purpose, we should choose a proper network as the auxiliary transformer. For convenient adjustment and compact structure, a low-pass network is applyed, as shown in Fig. 4. The matching feature of the network can be optimized flexibly by adjusting its components.

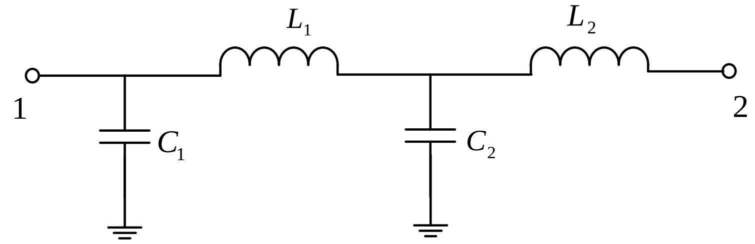


Fig. 4. Topology of low-pass network.

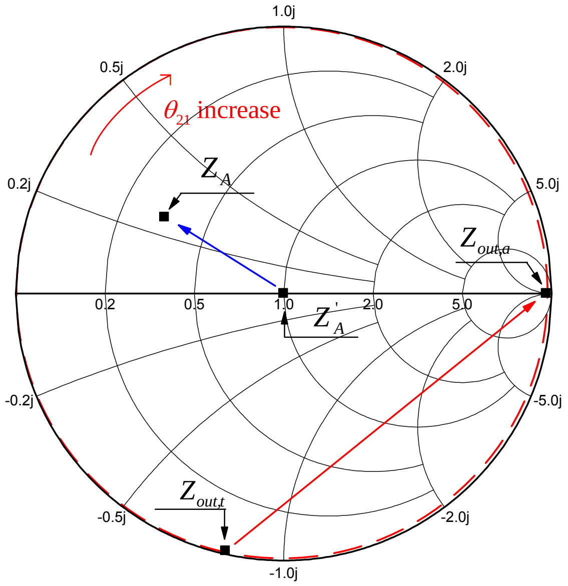


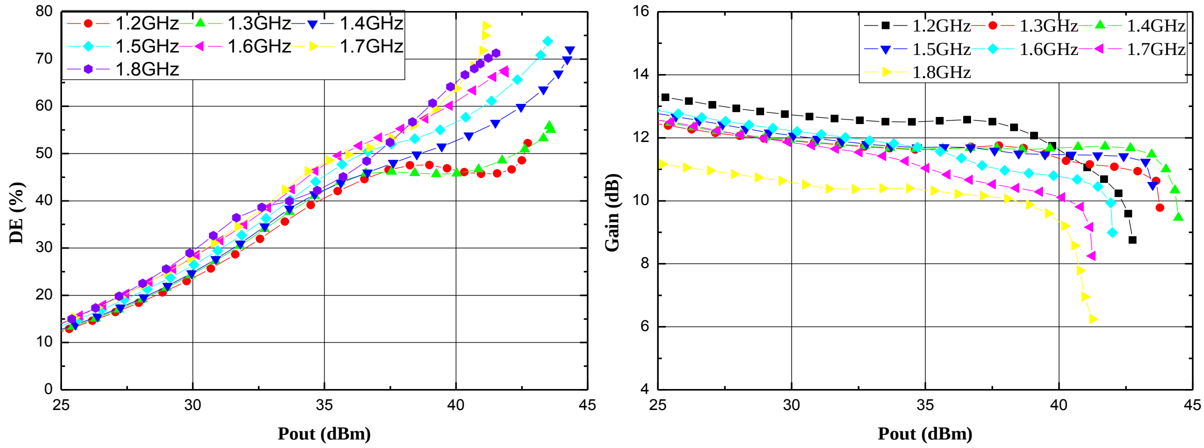
Fig. 5. Diagram of two-point matching of auxiliary transformer.

After the network's topology is selected, the components' value should be determined according to the requirement of impedance matching. Referring to [12], this work uses the two-point matching technique to design the auxiliary output matching network (OMN$_A$). Fig.5 shows the diagram of two-point matching. Considering the situation of peak power, we should choose appropriate value of the elements to transform $Z_A^{'}$ to Z_A, where $Z_A^{'}$ is the load impedance seen from the auxiliary transformer and Z_A is the load impedance seen from the auxiliary transistor. And Z_A should approach to the optimal load impedance for auxiliary transistor. It is remarkable that the output impedance of auxiliary transistor $Z_{out,t}$ lies on the edge of smith chart at back-off power. So an offset line is added near the power combination point. It is effective to change $Z_{out,t}$ to quasi-open circuit by tuning the offset line. While the offset line's characteristic impedance is equal to $Z_A^{'}$, the change of the length of the offset line will not affect the impedance matching at peak but affect the $Z_{out,a}$.

The output current relation between main and auxiliary devices has been stated in section II. For achieving proper current condition, we should precisely design the DPA's input part. A Wilkinson power divider was employed to split the input signal into two equal parts and then input power into the main and auxiliary device. The input matching networks (IMNs) is designed using low-pass type network to provide appropriate inputs for the two transistors within the desired bandwidth.

4. Simulation and Measurement

The harmonic balance simulations at the frequency range from 1.2 -1.8 GHz were performed to verify this design. According to the datasheet and the analyses in part II, the drain biases of carrier and peaking devices are set as 28 V and 32 V respectively. The gate biases of carrier and peaking device are -3 V and -5.4 V. The simulated drain efficiency (DE) versus output power is shown in Fig. 6(a) and the simulated gain versus output power is depicted in Fig. 6(b). Saturation output power is about 41.2 dBm - 44.4 dBm with the power gain of about 11.4 dB - 13.9 dB. It shows a 10-dB back-off efficiency of 32%-41% and a satisfactory saturated efficiency of 52%-76%.



(a) (b)

Fig. 6. (a) Simulated DE versus output power. (b) Simulated gain versus output power.

For further validation, the proposed DPA using Cree CGH40010F GaN HEMT was fabricated on a substrate Roger4003C with a thickness (h) of 0.813 mm and a dielectric constant (ε_r) of 3.38, as shown in Fig. 7. Fig. 8 (a) and Fig. 8 (b) give the performance of drain efficiency (DE) and gain respectively under continuous wave (CW) signal stimulation. The DPA is designed to operate from 1.2 GHz to 1.8 GHz, which corresponds to a 40% fractional bandwidth.

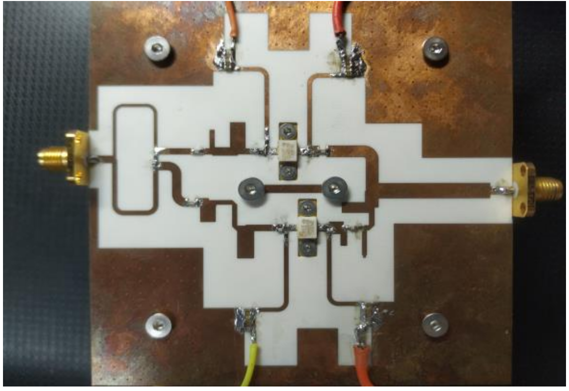
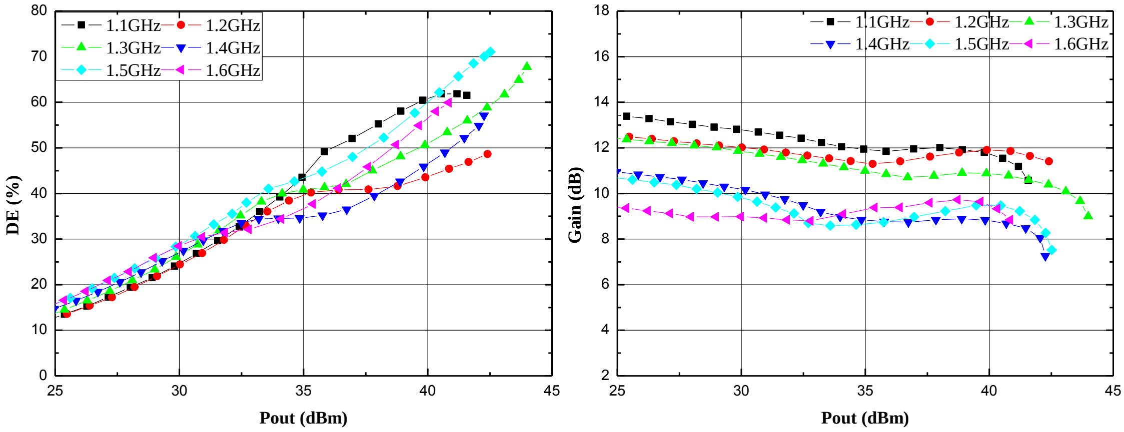


Fig. 7. Photograph of fabricated DPA.



(a) (b)

Fig. 8. (a) Measured DE versus output power. (b) Measured gain versus output power.

In the measurement, it was found to operate over the frequency range from 1.1 GHz to 1.6 GHz, about 37% fractional bandwidth. Degradation in bandwidth can be observed compared with the previous simulation results. It may be caused by the deviation of frequency features of the transistors. Its output power is about 41.0 dBm - 44.0 dBm at saturation, while the gain is about 10.0 dB - 13.5 dB. The measured DE at 10 dB back-off is between 30% and 40%, and the DE at saturation is about 48%-71%. In addition, obvious Doherty efficiency curve can be found in measured results.

The performances of this work and recent wide power back off range DPAs have been reported in Table I. [8] and [9] can sustain high efficiency only in a certain frequency and [10] has good performance just in narrow bandwidth. When compared to these works, the proposed DPA can exhibit broader operation bandwidth. It achieves good tradeoff between the high efficiency and wide bandwidth.

Table 1 Comparison with Some Related Doherty Amplifier

Ref	Frequency (GHz)	FBW (%)	Psat(dBm)	DE at 10-dB BO(%)	DE at saturation(%)
[8]	3.5	/	42.9	551	69
[9]	2.0	/2	42	60	64
[10]	1.6-1.9	17.1	42.5-43.0	46.0-46.3	78.3-83.0
This work	1.1-1.6	37	41-44	30-40	48-71

1. PAE at 9 dB POBO.

2. The bandwidth of 10-dB back-off DE performance hasn't been given out.

5. Conclusion

In this paper, a broadband Doherty power amplifier with extended power back-off range using two-section quarter-wave transformer is presented. The impedance transformation at back-off power and the choices of the characteristic impedances of the two transmission lines have been derived. The comparison between conventional case and maximally flat response case shows that the two-section transformer with maximally flat response characteristic can achieve broader matching bandwidth. The DPA which uses it can realize different load impedance transformations with different impedance ratios flexibly in broadband. Besides that, the band-pass auxiliary transformer can provide quasi-open circuit for main device at back-off power and achieve wider load modulation effect at peak power. For validation, the proposed amplifier was simulated, fabricated and measured. It can achieve considerable 10-dB back-off efficiency over a wide frequency band from 1.1 – 1.6 GHz.

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