Design and FPGA Implementation of LDPC Encoder Based on SRAA Algorithm

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Abstract

In order to improve the reliability of signal transmission, channel coding technology has become one of its effective measures, and LDPC code has become the best code type in channel coding today because of its excellent performance in medium and long codes. It has been wirelessly Widely used in communication, satellite communication and other fields. QC-LDPC code is an LDPC code with quasi-cyclic characteristics, which can greatly reduce the implementation complexity and has a good parallel implementation structure. The LDPC code in IEEE 802.11n is the QC-LDPC code, and the FPGA implementation structure of the LDPC encoder in the IEEE 802.11n standard is given based on the SRAA algorithm.

Keywords

LDPC; Encoder; SRAA; FPGA.

1. Introduction

Low-density parity-check (LDPC) codes are a class of linear error-correcting codes which claim a good performance for a large amount of data to be transmitted and stored in reliable condition[1]. Also, because of their block structure, they are suitable for hardware implementation. This work proposes a general type of unrolled layered LDPC decoding architectures which are meant to be included in the telecommunication standards (5G standard, WiMAX [2], DVB-S2 [3], Wi-Fi [4]).

LDPC codes were discovered in 1960 by Robert Gallager. research period,where he gave also a powerful bounding technique to assess and evaluate the maximum-likelihood performance of coding systems as stated in [5]. But because of their major complexity in implementation (compared to their performance expectation) together with the technology whichexisted in that period, their actual "optimal" implementation was lacking a good support. Untilin 1990s, when turbo codes were rediscovered, LDPC codes were totally ignored. After that,the study of good data transmission and storage was continued by emerging the iterative decoding algorithm in the coding schemes. Here is where LDPC codes became known for their performance, which was close to the Shannon's limit, and in the same time having an acceptable complexity vs throughput ratio.

LDPC codes are suitable for hardware implementation due to their linear block structure. Also, in industry, for the actual implementation of the decoder, it is used the iterative message-passing decoding algorithm (known also as belief propagation or sum-product algorithm; will be used further on as belief propagation). A good throughput(few tens of Gbps) can be obtained by a implementing a certain class of belief propagation algorithms.Because of its parallelization structure, the decoding algorithm can be easily designed and implemented on an FPGA (Field Programmable Gate Array) device.

2. LDPC Coding Algorithm

2.1 The Main Coding Algorithm

LDPC coding algorithms mainly include RU coding algorithm, direct coding algorithm and SRAA algorithm. Neither the RU encoding algorithm nor the direct encoding algorithm can simultaneously satisfy low hardware complexity and bit rate compatibility. The arithmetic unit in the direct coding

algorithm has a high correlation with the code rate, and is easy to code rate compatible with the structural design of the encoder, but its hardware implementation complexity is high. However, the direct coding algorithm does not use the quasi-cyclic structure of QC-LDPC codes. The unit quasi-cyclic characteristics of QC-LDPC codes in 802.11n can greatly simplify the direct coding algorithm. SRAA is one of the more classic algorithms.

2.2 SRAA Algorithm

The QC-LDPC code is a quasi-cyclic structure. The unit quasi-cyclic characteristics of the QC-LDPC code in the 802.11n protocol can greatly simplify the direct encoding algorithm. The SRAA algorithm is one of the more classic algorithms.

Define the check code generated after encoding as **p**, then:

$$\mathbf{p} = \begin{bmatrix} \mathbf{p}_0 & \mathbf{p}_1 & \cdots & \mathbf{p}_{M-1} \end{bmatrix} \tag{1}$$

The rule for dividing the check code is related to the expansion factor Z of the H-based matrix. Taking the QC-LDPC code with 1944 code length in 802.11n as an example, the sub-vector size in equation (1) is Z=81, then:

$$\mathbf{p} = XP^T = \begin{bmatrix} XG_0 & XG_1 & \cdots & XG_j & XG_{M-1} \end{bmatrix} = \begin{bmatrix} \mathbf{p}_0 & \mathbf{p}_1 & \cdots & \mathbf{p}_j & \mathbf{p}_{M-1} \end{bmatrix} \tag{2}$$

Here, the information bit part of length k is divided into blocks of Z length as follows:

$$X = \begin{bmatrix} \mathbf{x}_0 & \mathbf{x}_1 & \cdots & \mathbf{x}_{K-1} \end{bmatrix} \tag{3}$$

Here, $\mathbf{x_p} = \begin{bmatrix} x_{(p-1)z} & x_{(\rho-1)Z+1} & \cdots & x_{pZ-1} \end{bmatrix}$,from formula (2) and formula (3), we can get:

$$\mathbf{p_j} = \mathbf{x}_0 G_{0,j} + \mathbf{x}_1 G_{1,j} + \cdots + \mathbf{x}_{K-1} G_{K-1,j} \tag{4}$$

Since G_{ij} is quasi-cyclic, here can use its quasi-cyclic characteristics to transform formula (4). Definition $\mathbf{g}_{\rho,j}$ is the first row of the $G_{\rho,j}$ sub-blocks, which is also called the generator of $G_{\rho,j}$. The other rows of this sub-block can be represented by the cyclic shift of the generator. Define $r(x)$ to rotate right by x bits. Take item ρ in formula (4) as an example:

$$\mathbf{x_p} G_{\rho,j} = x_{(\rho-1)Z} \mathbf{g}_{\rho,j}^{r(0)} + x_{(\rho-1)Z+1} \mathbf{g}_{\rho,j}^{r(1)} + \cdots + x_{\rho Z-1} \mathbf{g}_{\rho,j}^{r(Z-1)} \tag{5}$$

It can be seen from equation (5) that in the encoding operation of each sub-item in (4), Just need to know $\mathbf{g}_{\rho,j}$. In the hardware implementation, there is no need to store the complete $G_{\rho,j}$ matrix, and the storage space becomes 1/Z of the direct encoding algorithm, which greatly saves the hardware storage space. According to formula (5), the circuit structure of $\mathbf{x_p} G_{\rho,j}$ is shown in Figure 1.

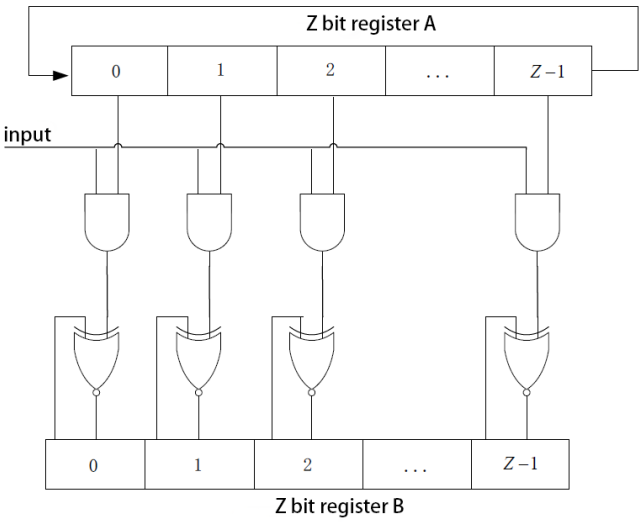

Fig. 1 SRAA algorithm logic circuit diagram

Equation (5) corresponds to the hardware circuit. The Z bit data of $\mathbf{g}_{\rho,j}$ is stored in register A. A group of shift registers is used to replace the original $G_{\rho,j}$ matrix that needs to be stored. The entire circuit performs a shift-add operation, and the operation result $\mathbf{x}_\mathbf{p}G_{\rho,j}$ is stored in register B. Therefore, the algorithm corresponding to formula (5) is called SRAA (Shift Register Adder Accumulator) algorithm.

3. FPGA Implementation and Modelsim Simulation

The encoder uses 27-bit parallel input and 27-bit parallel input. The main module of the encoder is the data path unit of the control module and the encoder. The main function bits of the control module control the data input; the function of the data path unit is for data deal with. The integrated RTL diagram is shown in Figure 2:

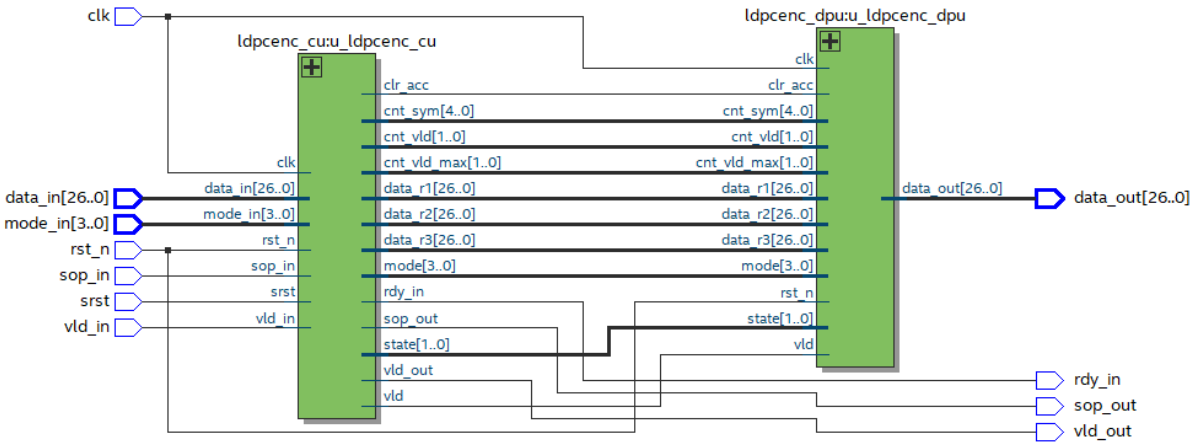

Fig. 2 Encoder RTL synthesis diagram

Modelsim simulation input is 1620-bit data, and output is code length 1944-bit data. The simulation data of FPGA encoder is verified in Matlab. The results are consistent, indicating that the circuit is working normally. The encoder simulation diagram is shown in Figure 3:

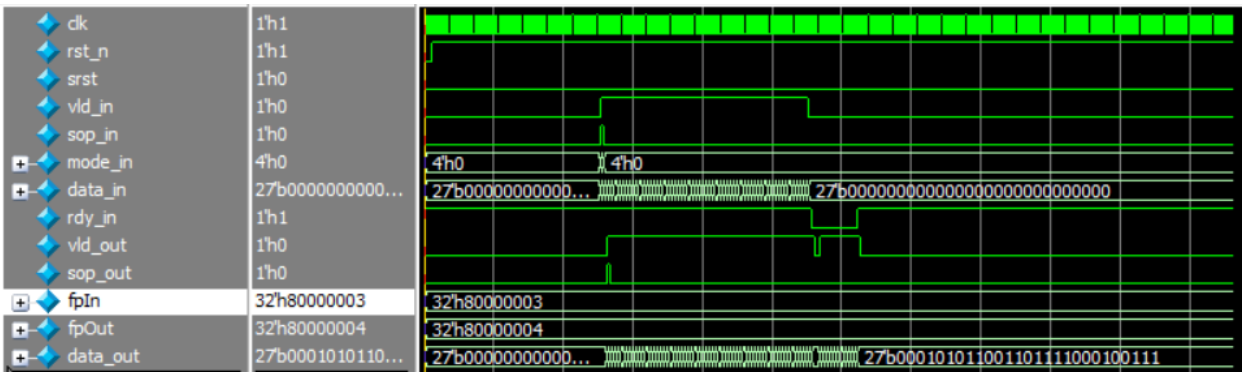

Fig. 2 Encoder simulation timing diagram

FPGA resource occupation is shown in Table 1:

Table 1 Encoder synthesis results

Resource	Logic utilization (in ALMs)	Total registers	Total pins
Number	5,516 / 56,480 (10 %)	1706	66 / 268 (25 %)

4. Summary

This paper uses FPGA to implement the LDPC encoder in the IEEE802.11n standard, based on the SRAA algorithm. The encoder can be used in WiFi systems.

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